

## PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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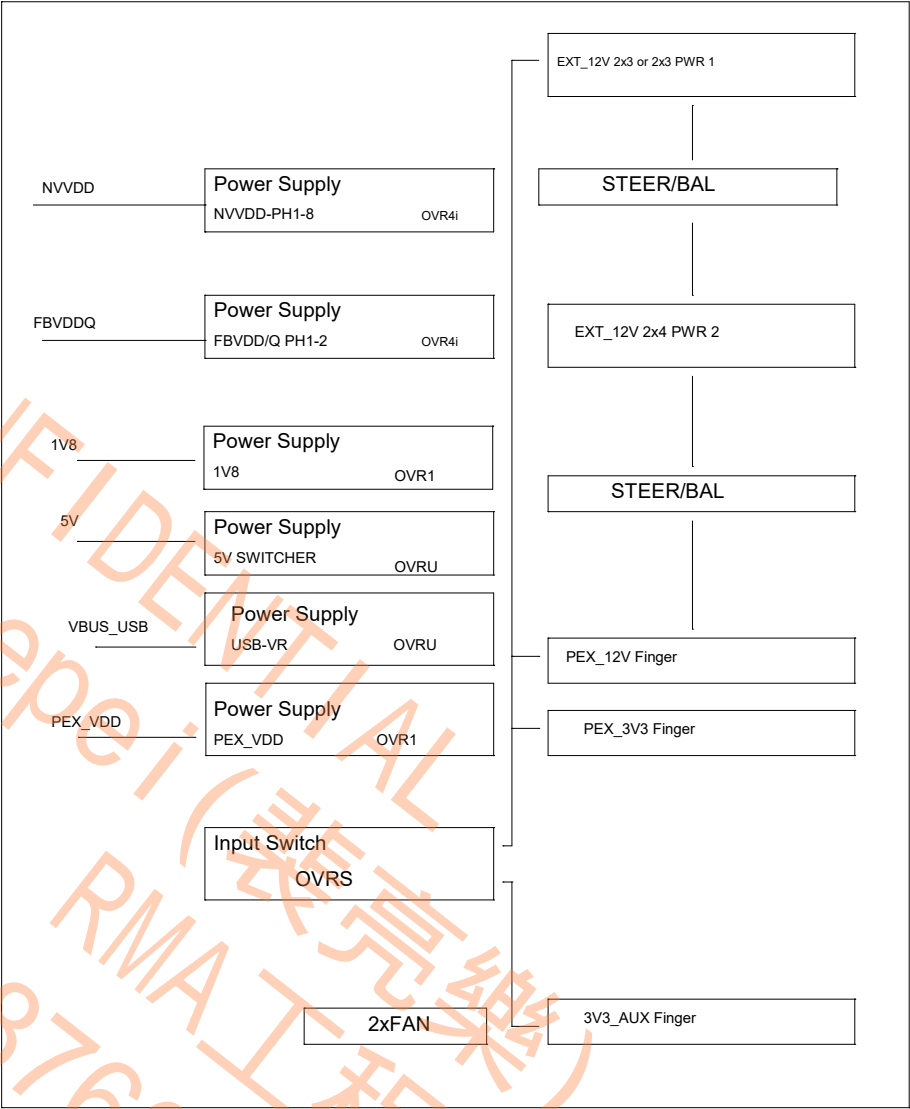
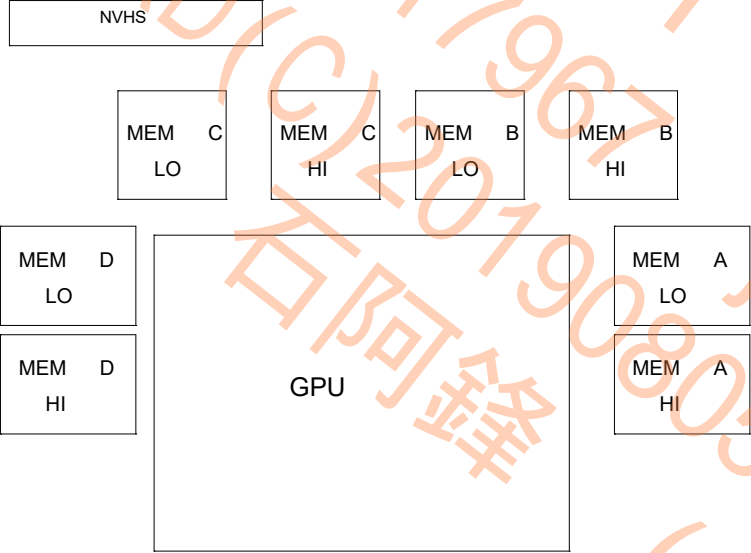
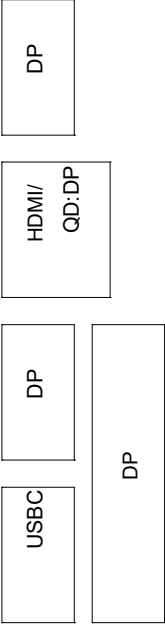
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42	PS: 12V CURRENT STEERING
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V372-3.0 change List
18 Change J4 footprint
19 Change J3 footprint
20 Remove DP co-layout
21 Remove JTAG & unused GPIO
32 Remove 0031_PS_FBVDD CONTROLLER OVR3
34 NVVDD CONTROLLER change to MP2888A
35 DRMos change to 10phases
36 DRMos change to 10phases
37 Add NVVDD Output CAP
41 Remove INPUT SWITCH Rail Balance
44 J8 change to 8pin
Add Fuse F1~F3
Change 12V input choke footprint
45 Add Hot Unplug Detect for J8
52 Add Remove LED & Fan Vin_12V option
53 Add MCU IT8295 for RGB LED

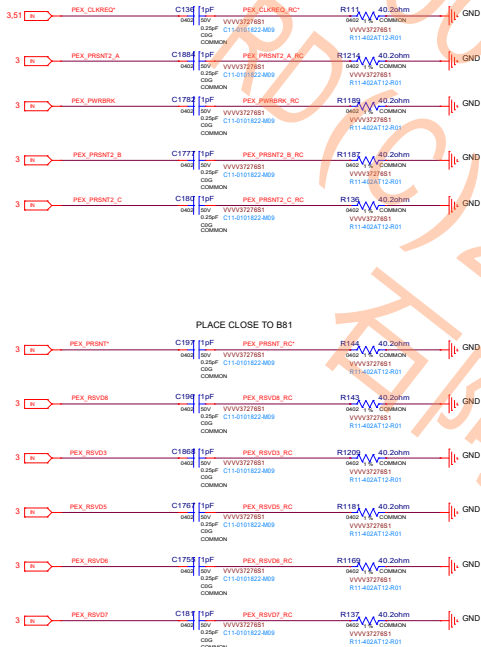
V372-3.1 change List
Base on V372-3.0 · No changed

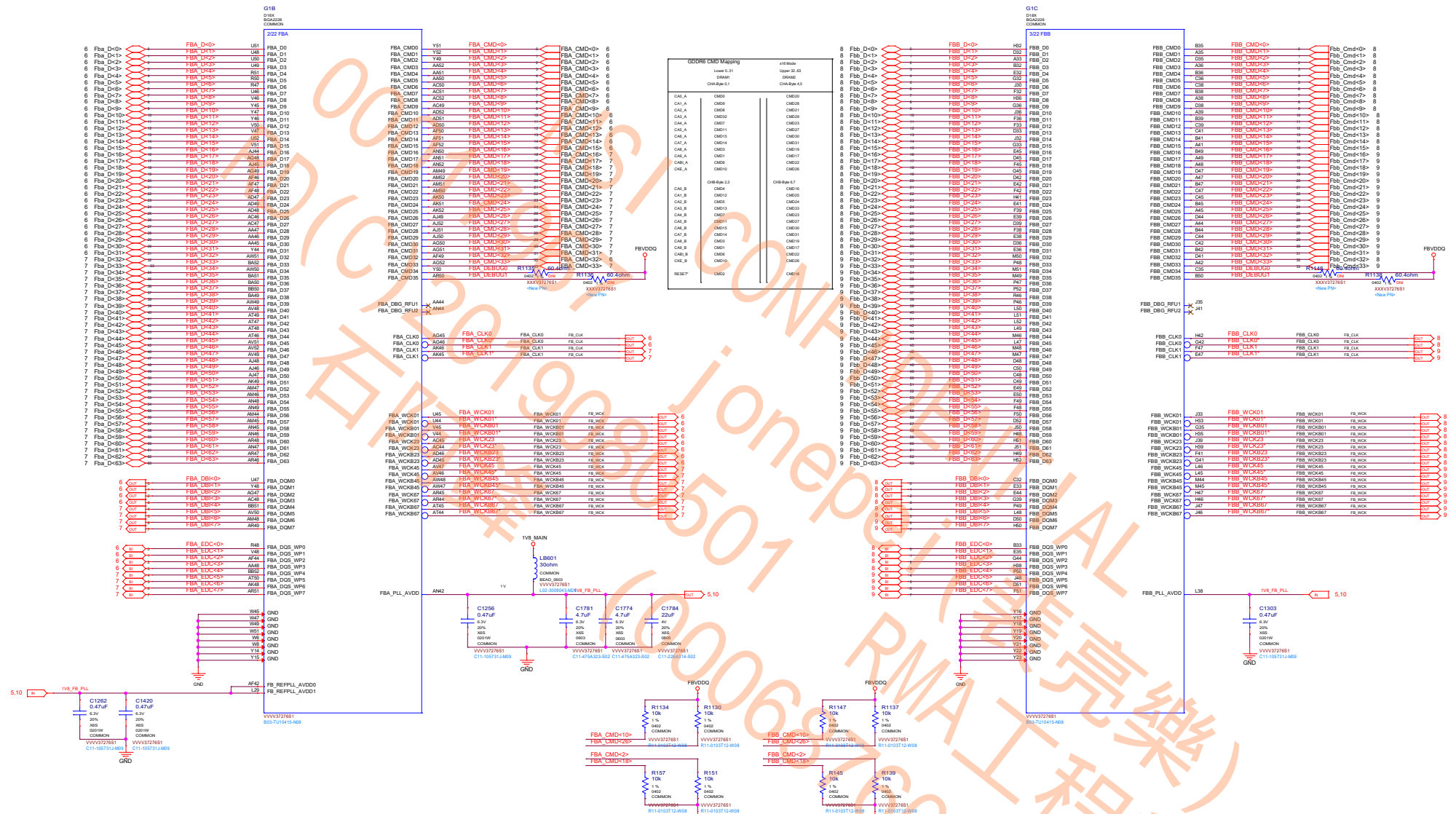
V372-3.2 change List
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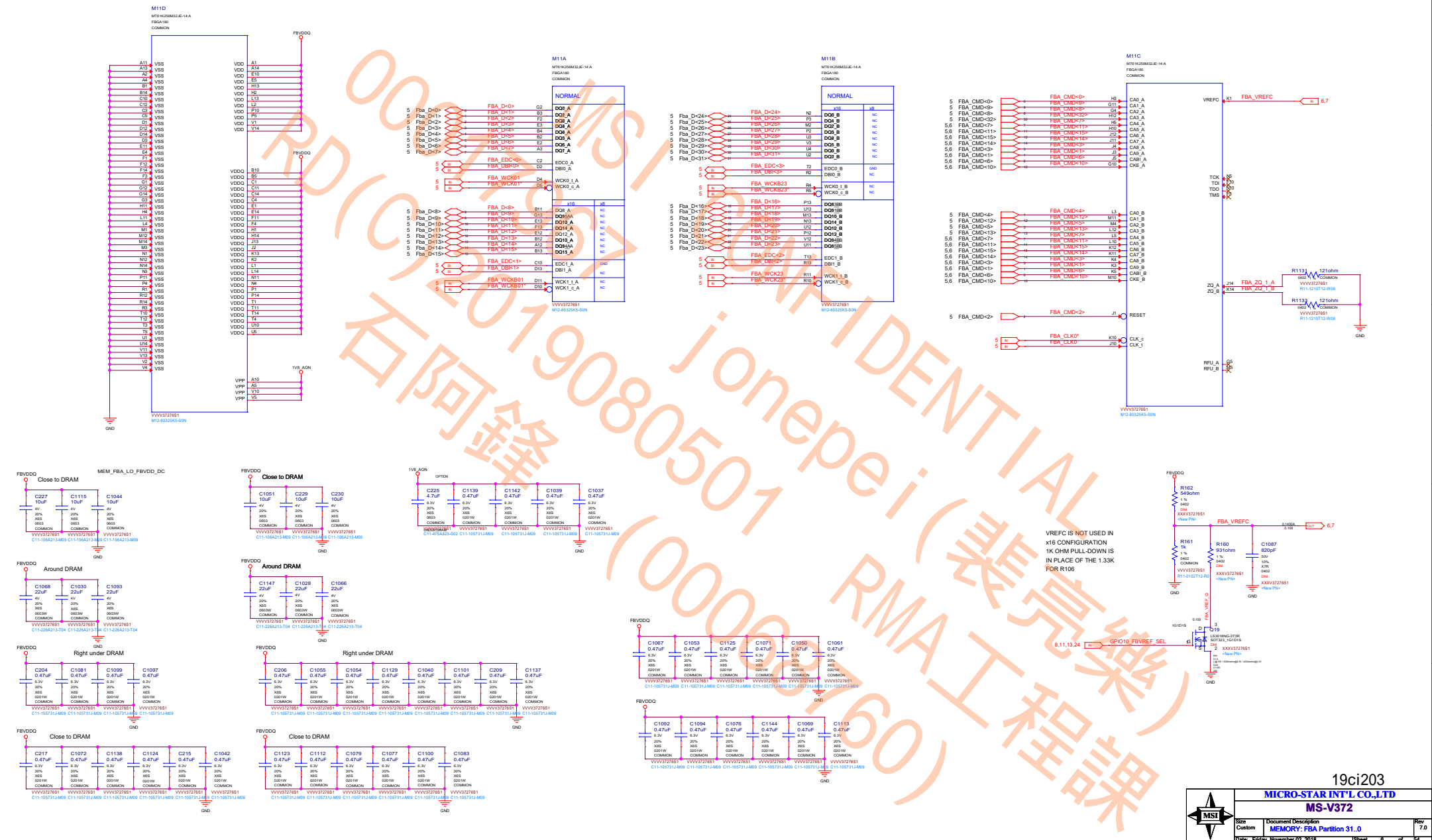
V372-3.0 change List
3 Remove I2CS · PEX_WAKE* · POWER_BRAKE* · 3V3_AUX_CON
19 Add DP_PWR bypass resistor
C12 changed to 560uF Solid CAP
22 Remove HDMI co-layout
C15 changed to 560uF Solid CAP
23 Remove SLI_BRG_PRST*
24 Remove POWER_BRAKE* · Unused GPIO
29 Add MP1475DJ for 5V Schematics
31 FBVDD controller changed to uP1666QQKF
33 FBVDD MO changed to UBIQ/QN3103M6N+QN3107M6N
34 NVVDD controller changed to MP2886A
35 Change NVVDD phase1-6
36 Remove NVVDD phase8-10
37 Remove some NVVDD output CAPs
39 Remove INPUT SWITCH RTD3
40 Remove INPUT SWITCH RTD3 USB
41 Remove INPUT SWITCH Rail Balance
43 Remove VR THERMAL PROTECTION
44 J8 changed to 6pin
Remove INA3221 · 3V3_AUX_FUSE
47 Remove GPIO1_GC6_FB_EN · 1V8MAIN ENABLE
Remove NV3V3 BACKUP SOLUTION
44 Remove SLI_BRG_PRST* · PS_1V8_AON_EN · THERM_OVERT*
Remove PS_SLI_FGC6_OR · PS_FBVDD_BUFF_R
49 Remove GPIO1_GC6_FB_EN · PS_RTD3_12V_SW
Remove 12V Voltage Monitor
51 Remove PEX_WAKE
53 Remove LED_CONTROLLER_IT8295



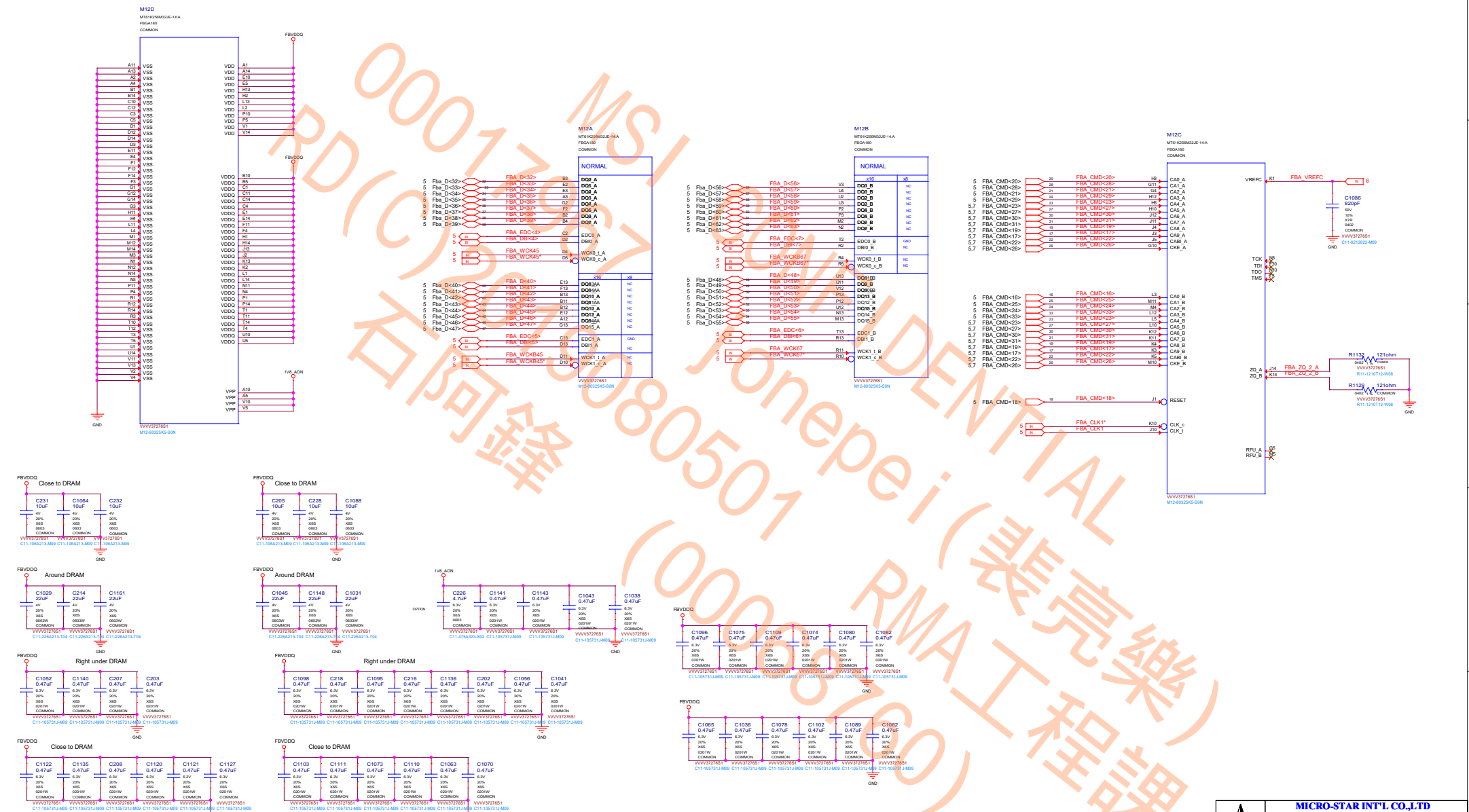








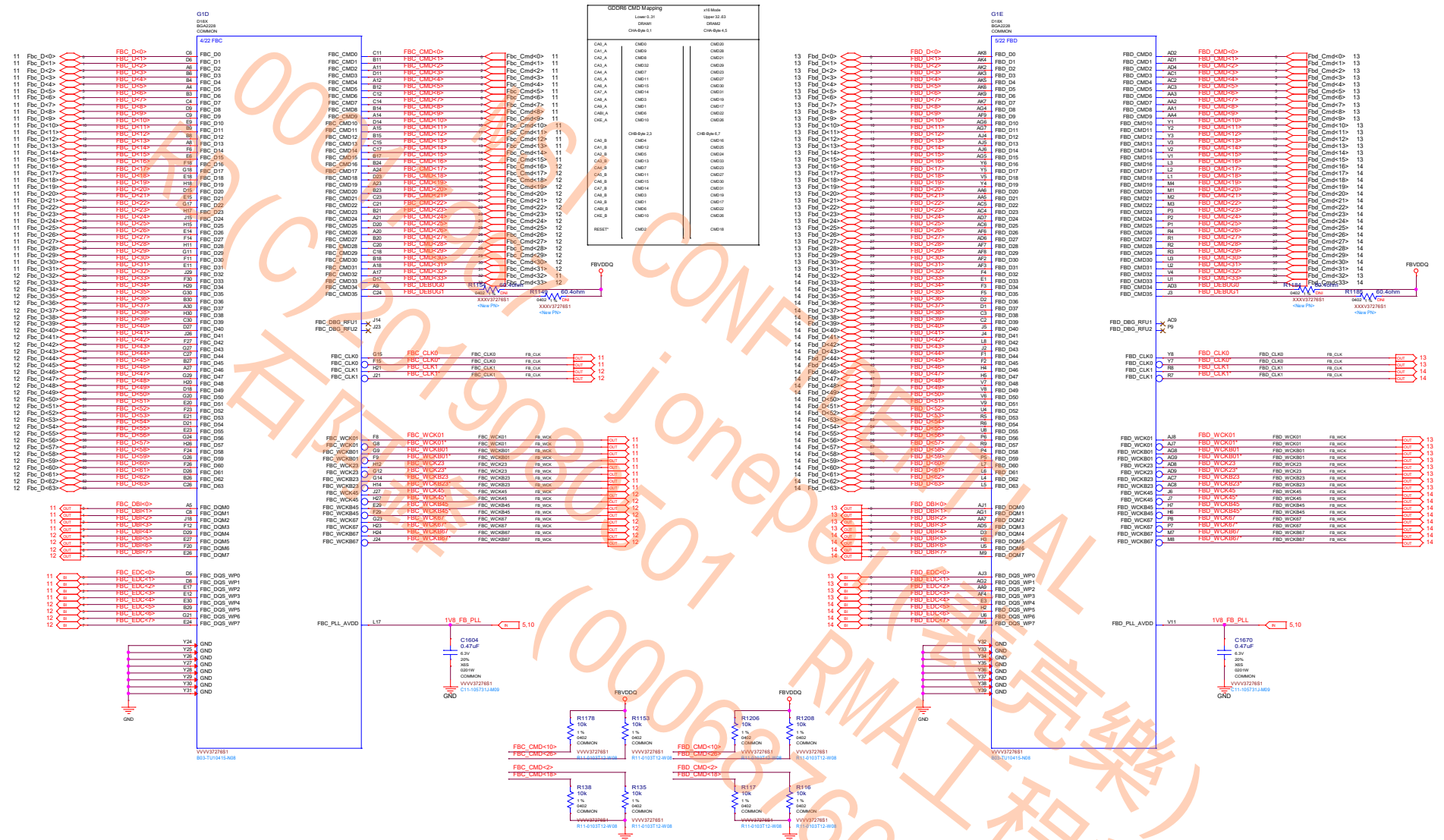


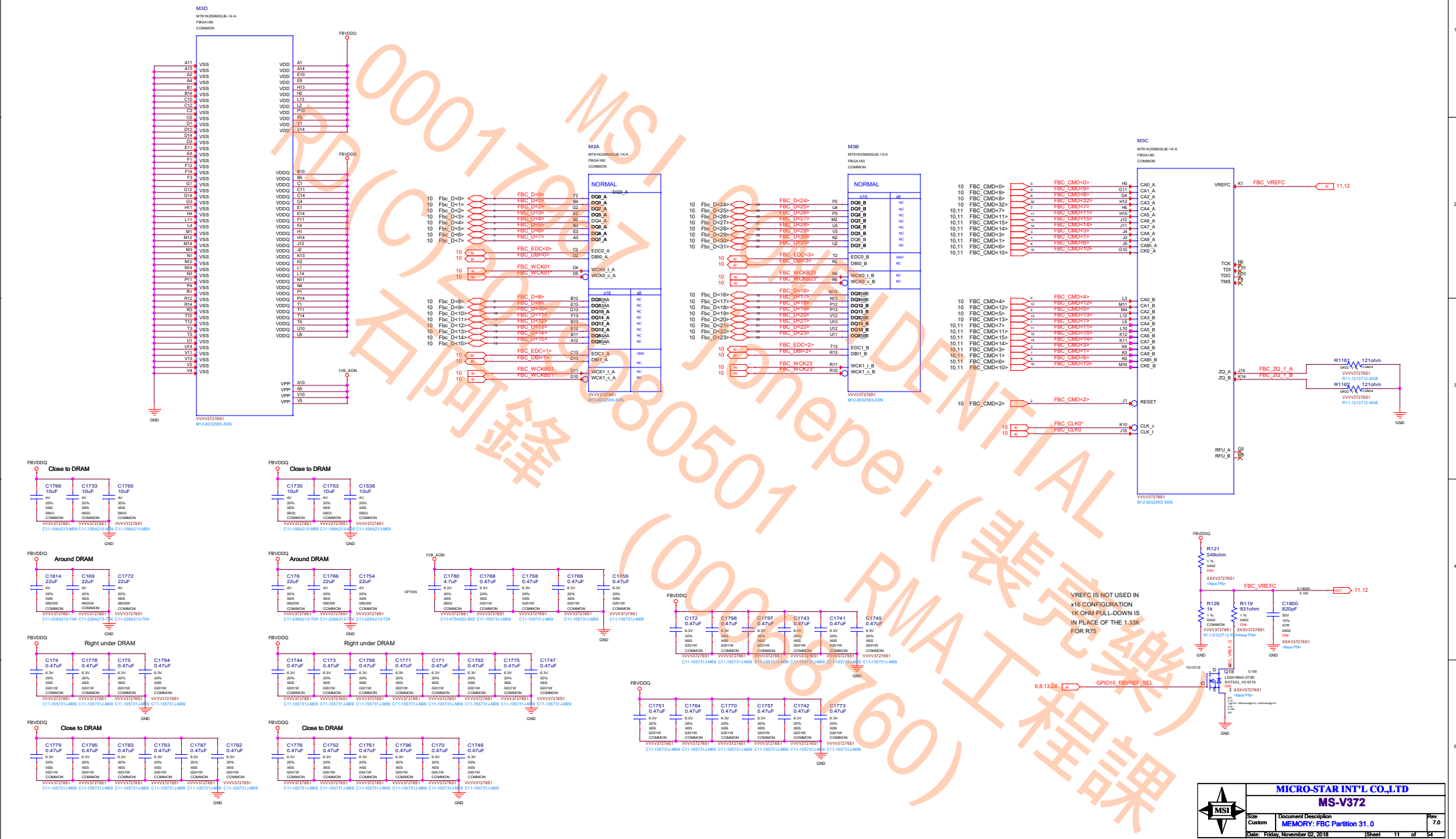


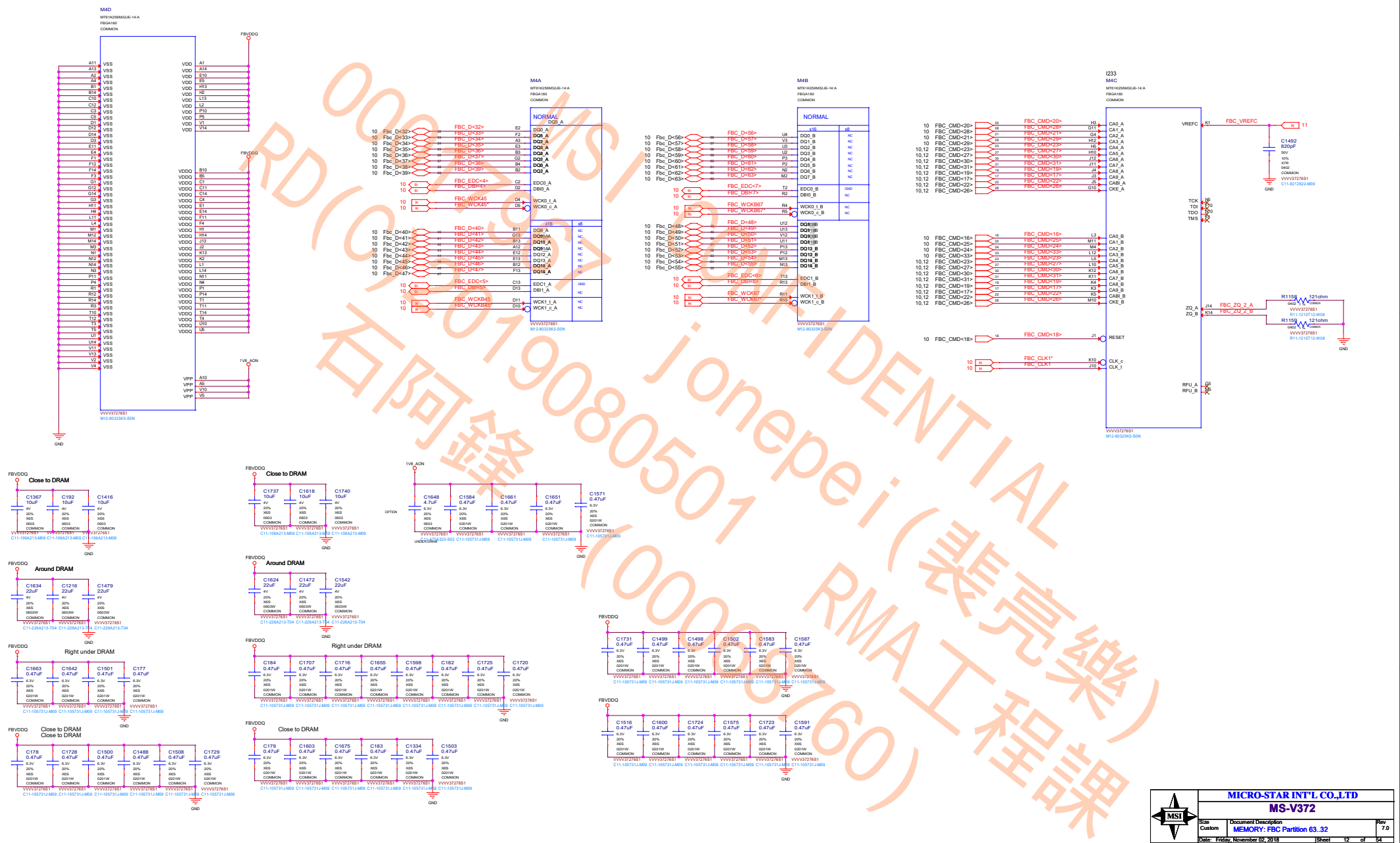


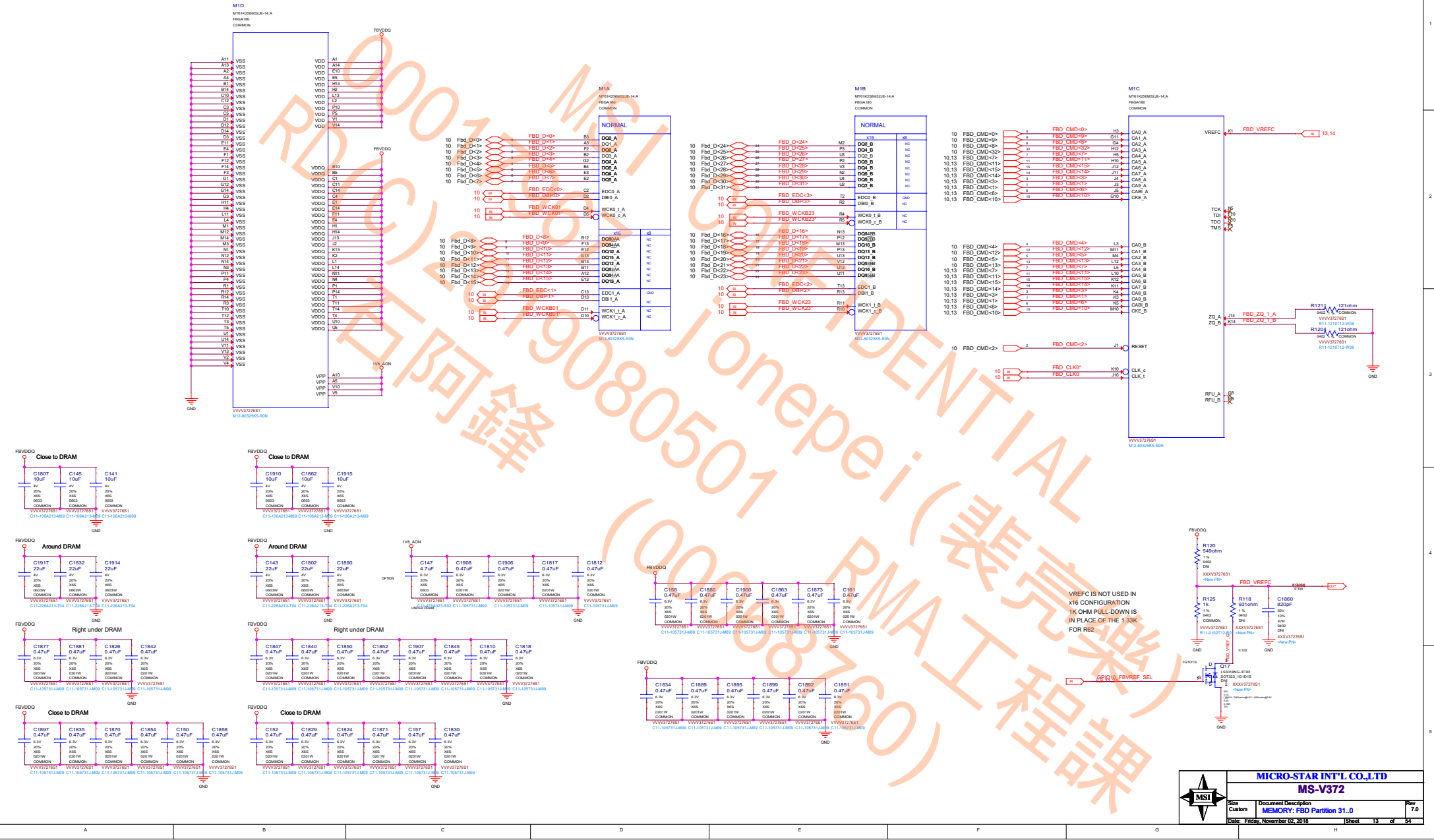




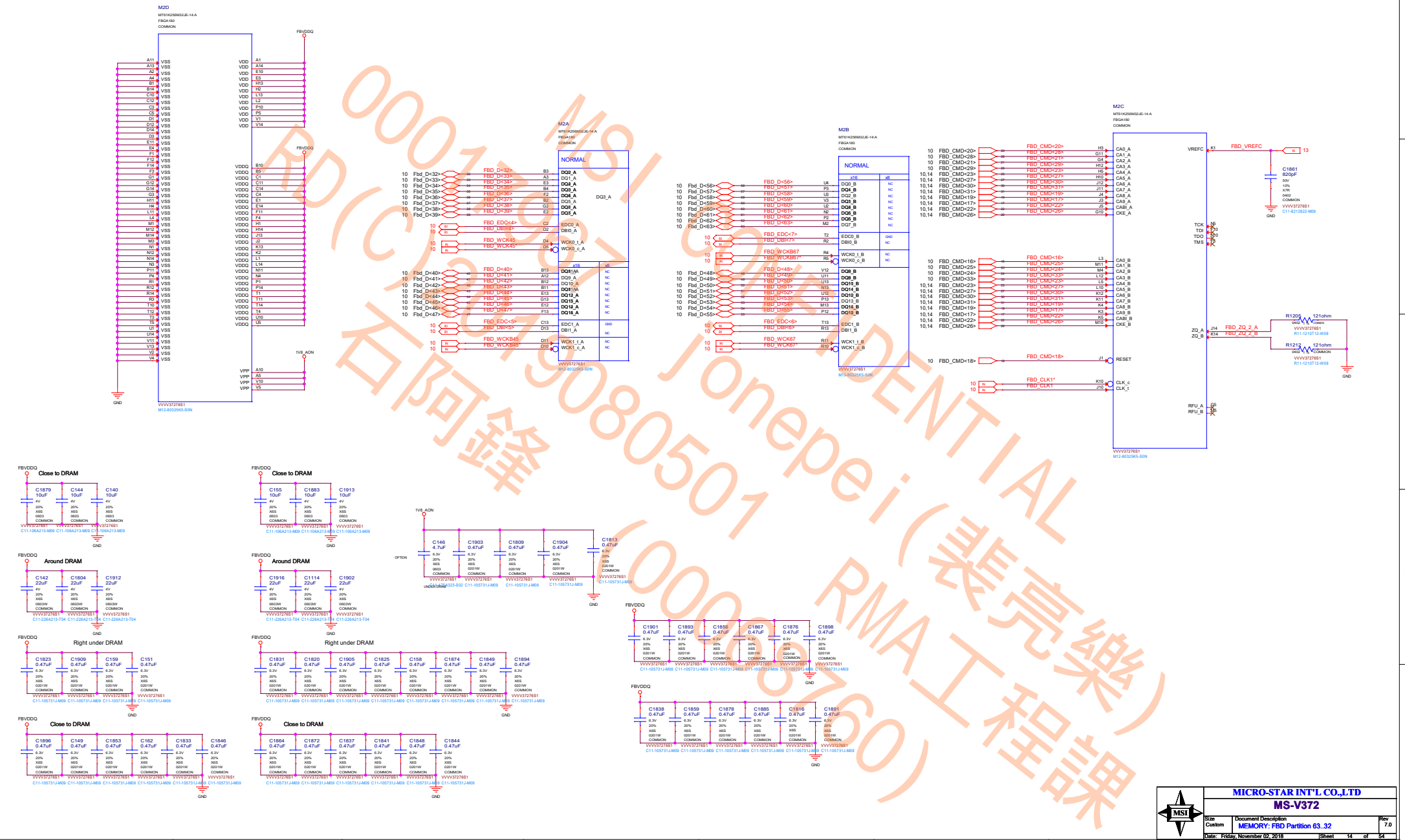












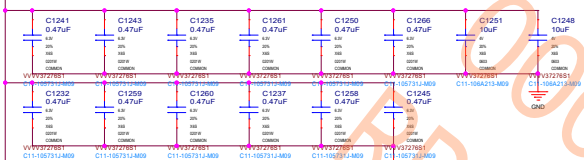




## NVVDD

## FBVDDQ

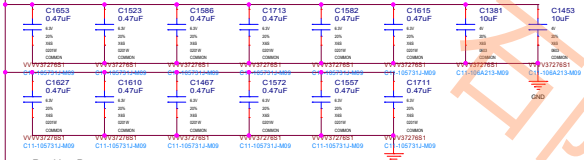
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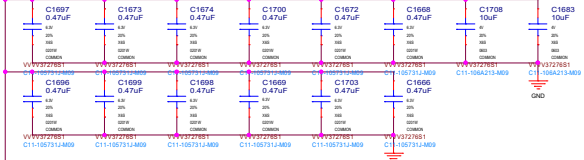
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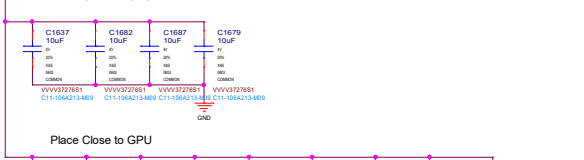
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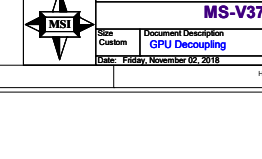
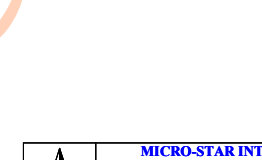
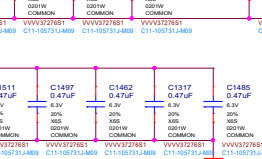
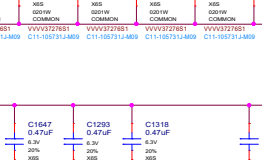
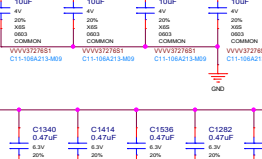
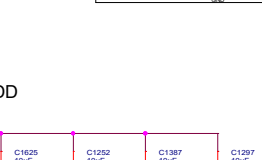
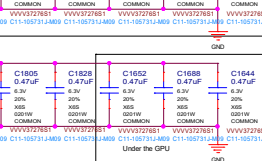
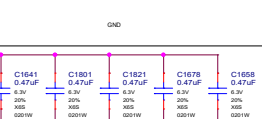
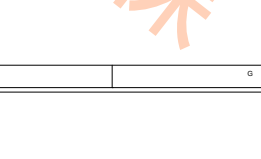
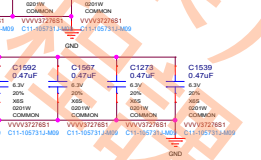
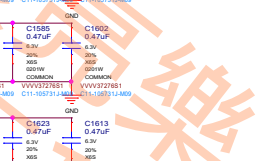
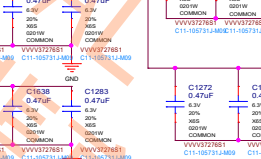
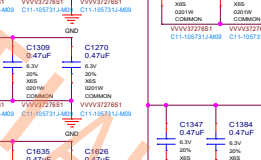
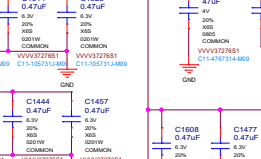
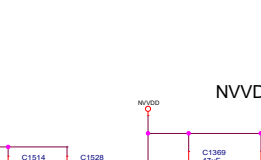
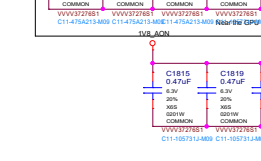
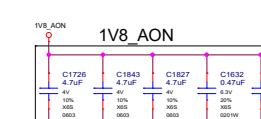
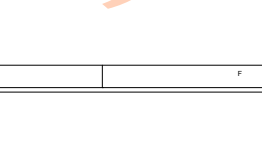
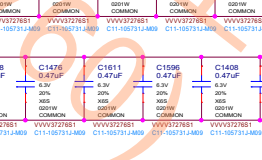
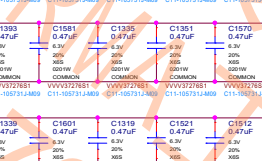
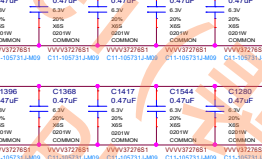
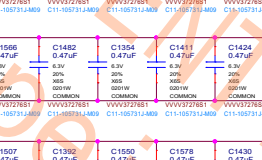
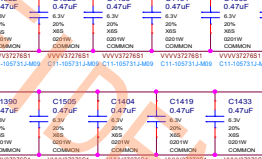
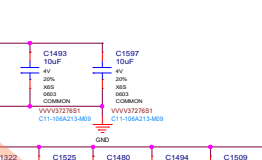
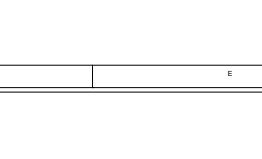
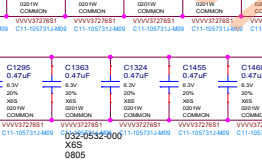
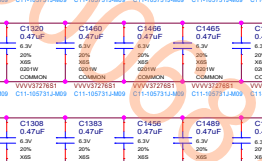
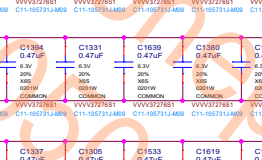
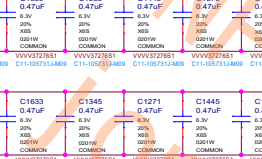
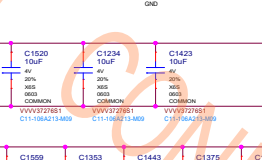
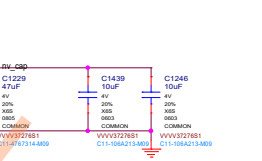
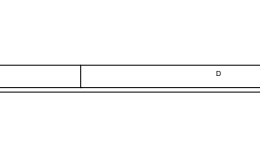
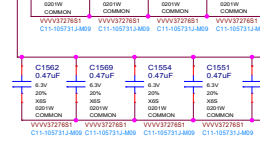
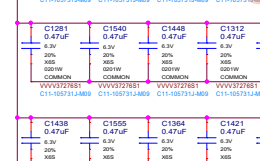
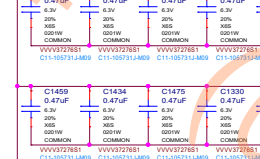
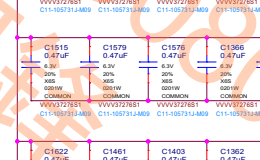
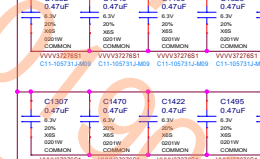
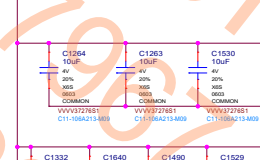
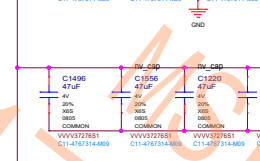
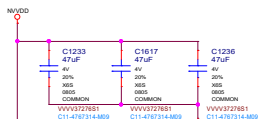
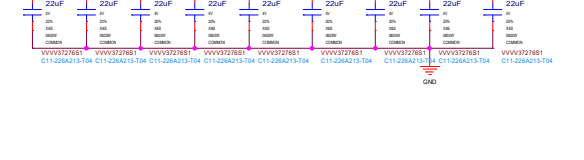
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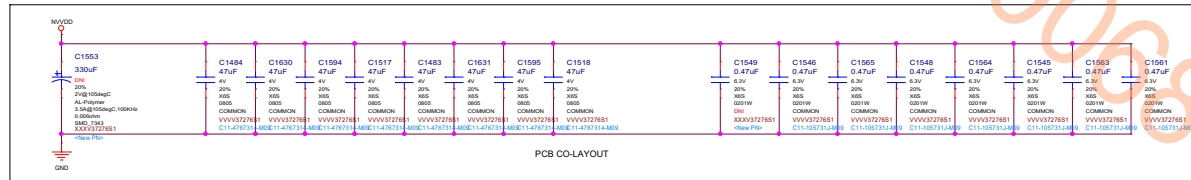
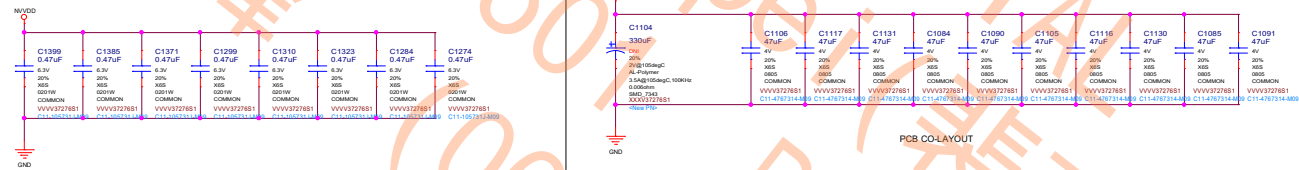
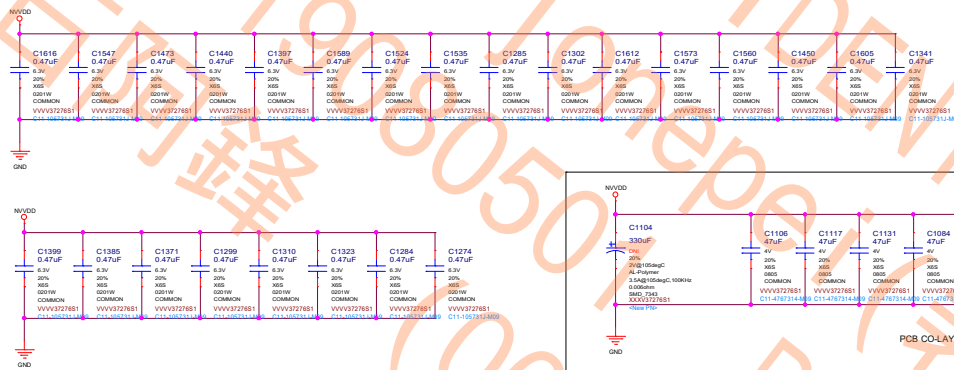
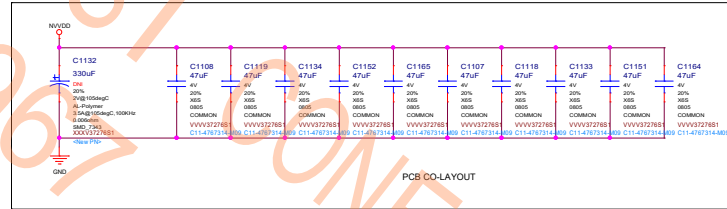
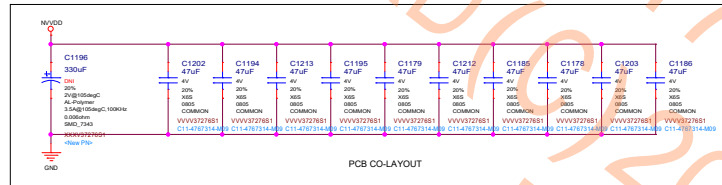
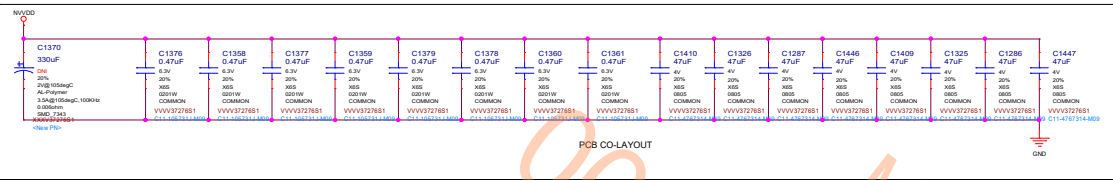


## Place Close to GPU



## Place Close to GPU



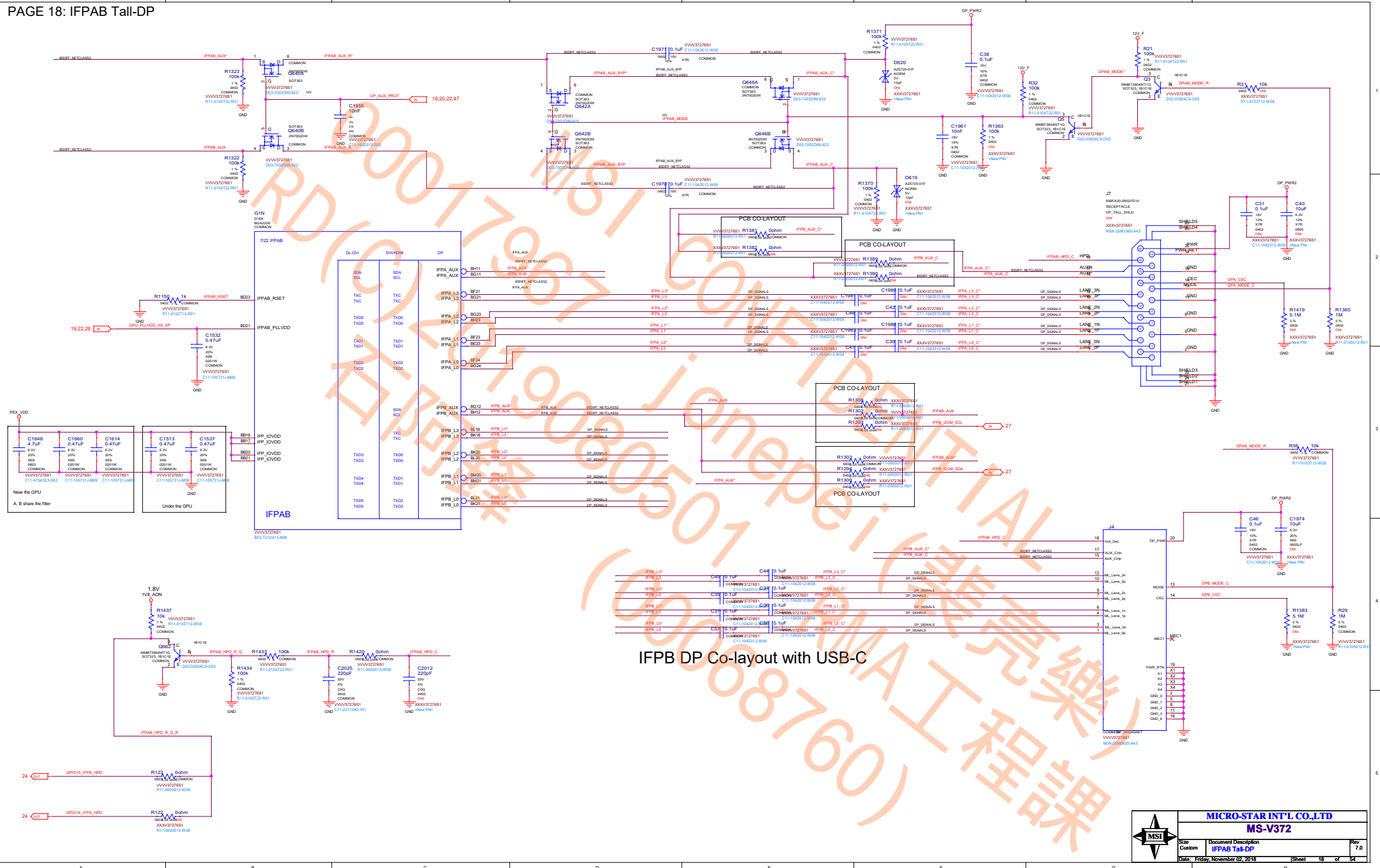


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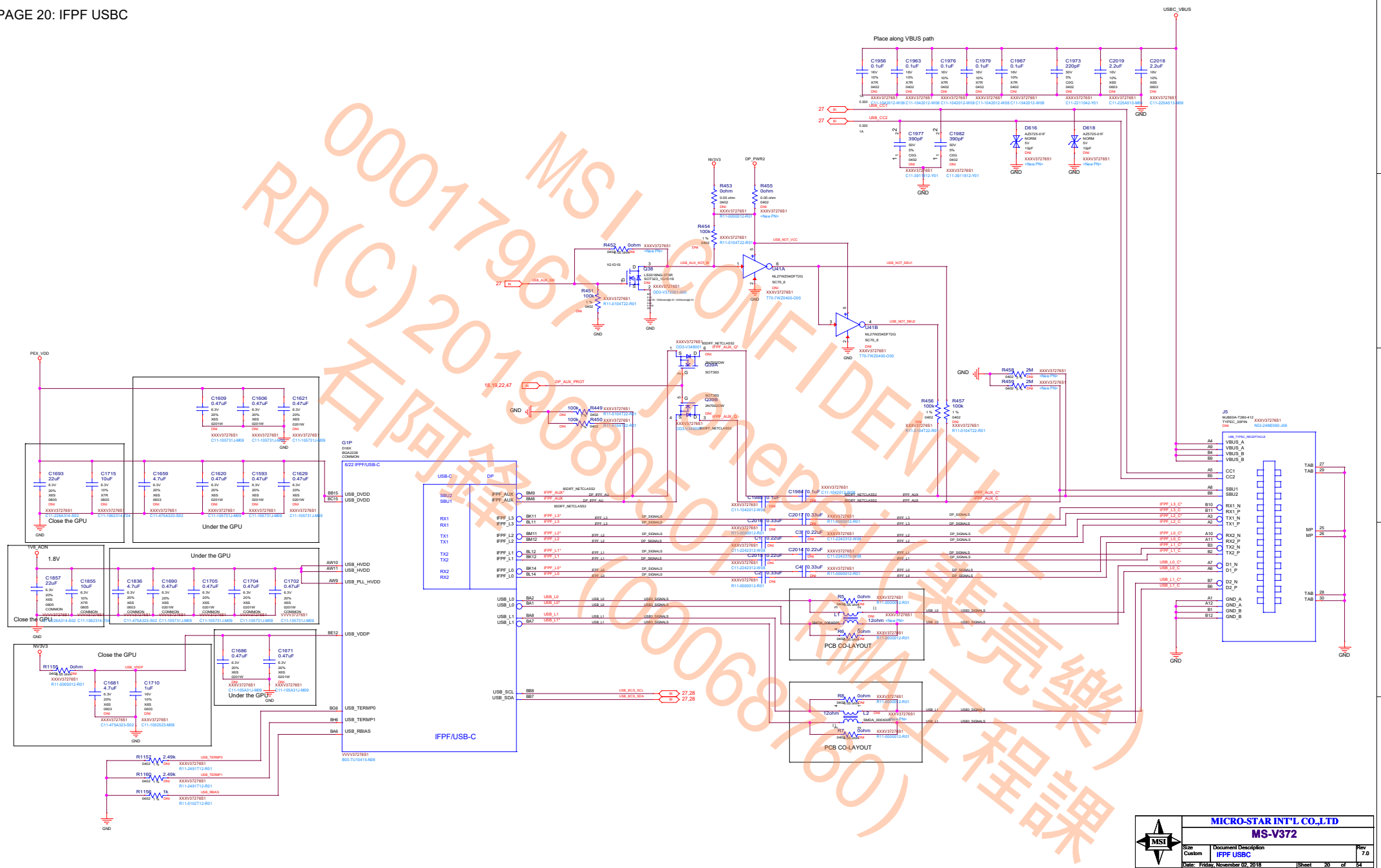
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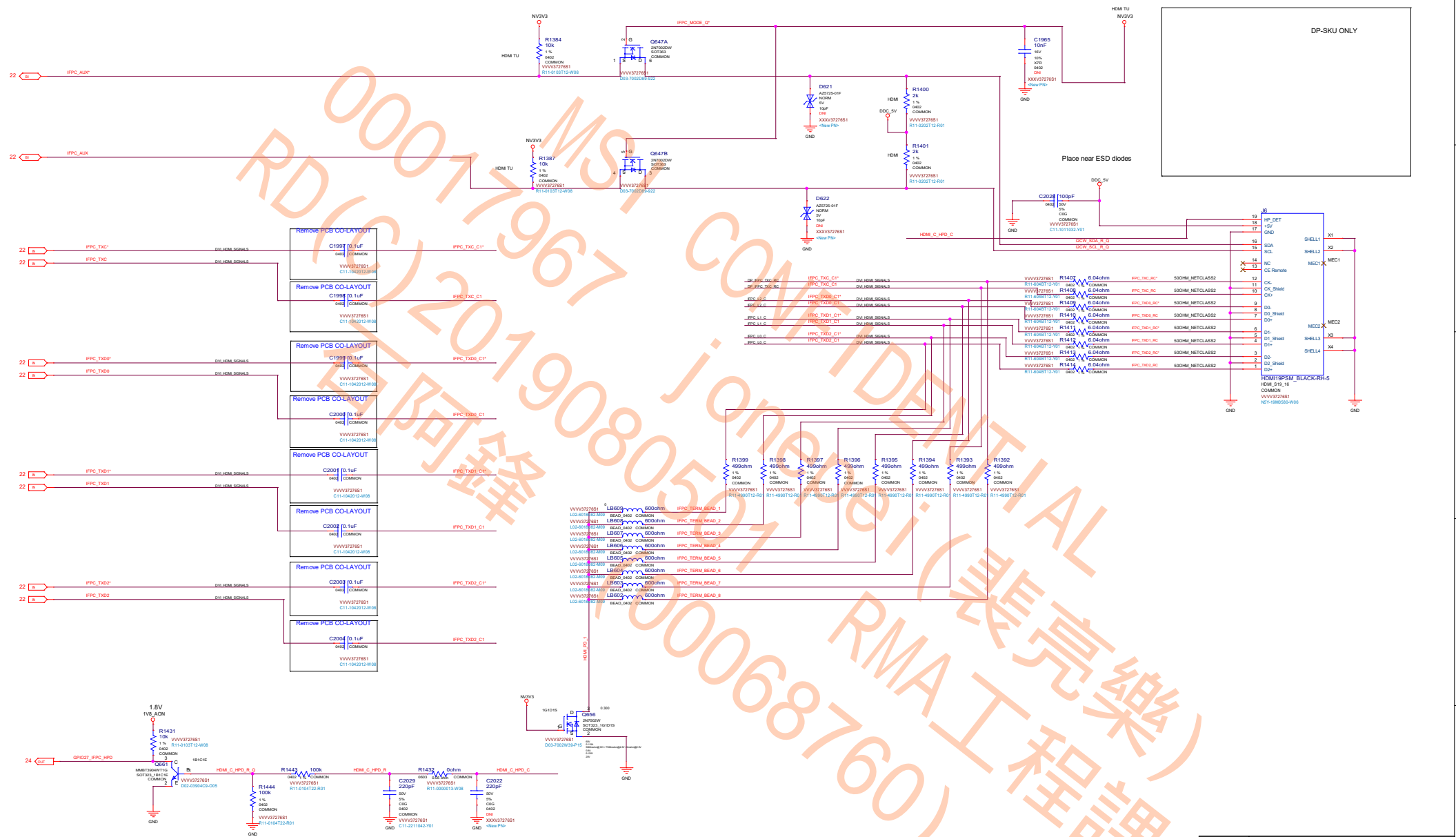




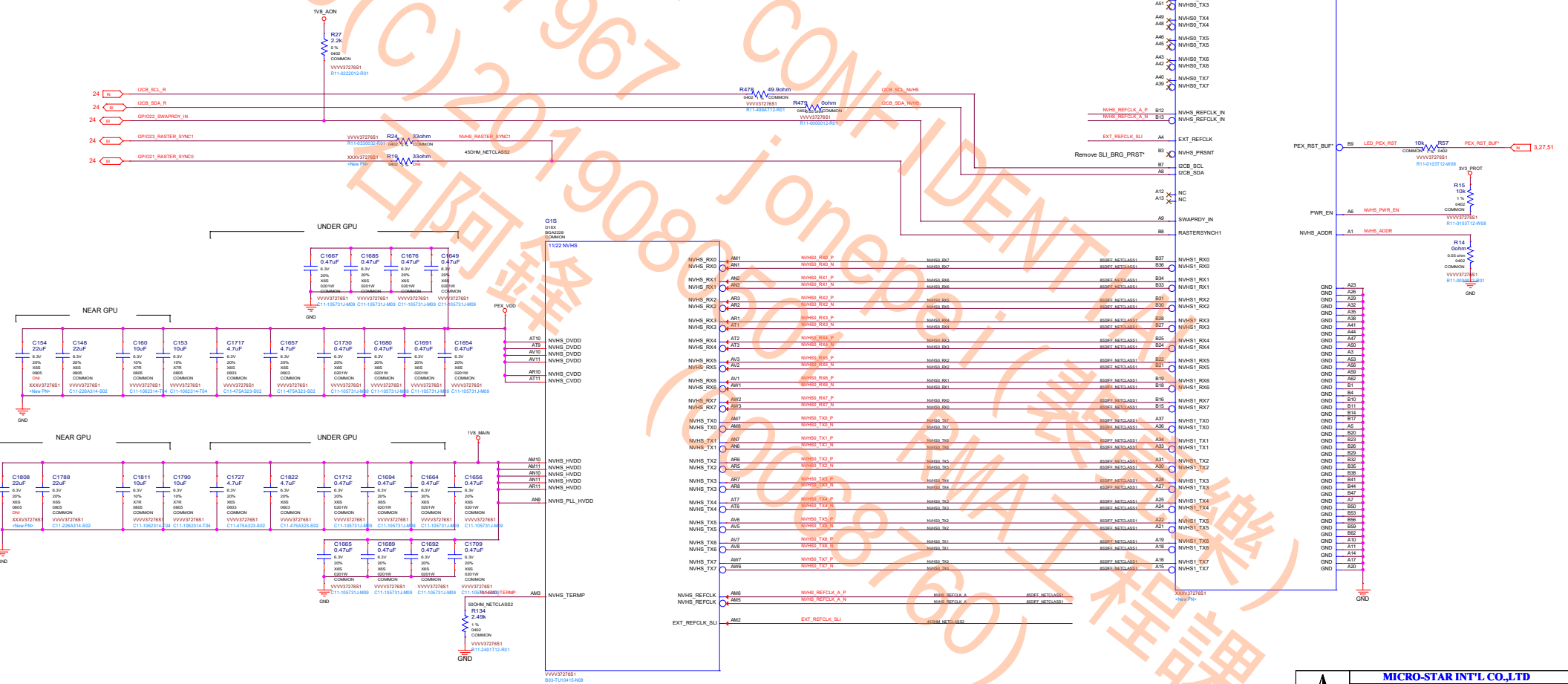
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H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	1:ENABLE 0:DISABLE FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

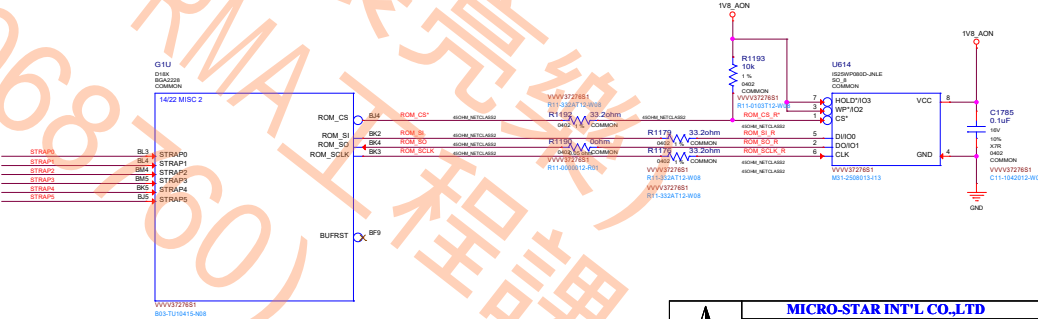
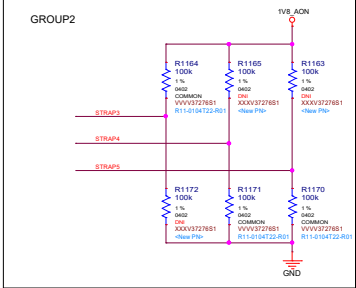
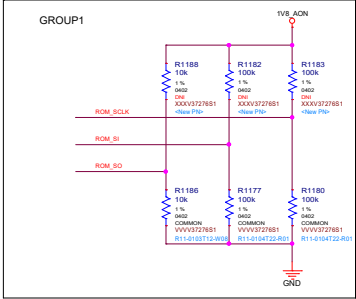
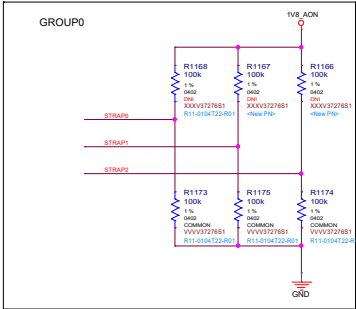
DEFAULT

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M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



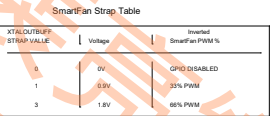


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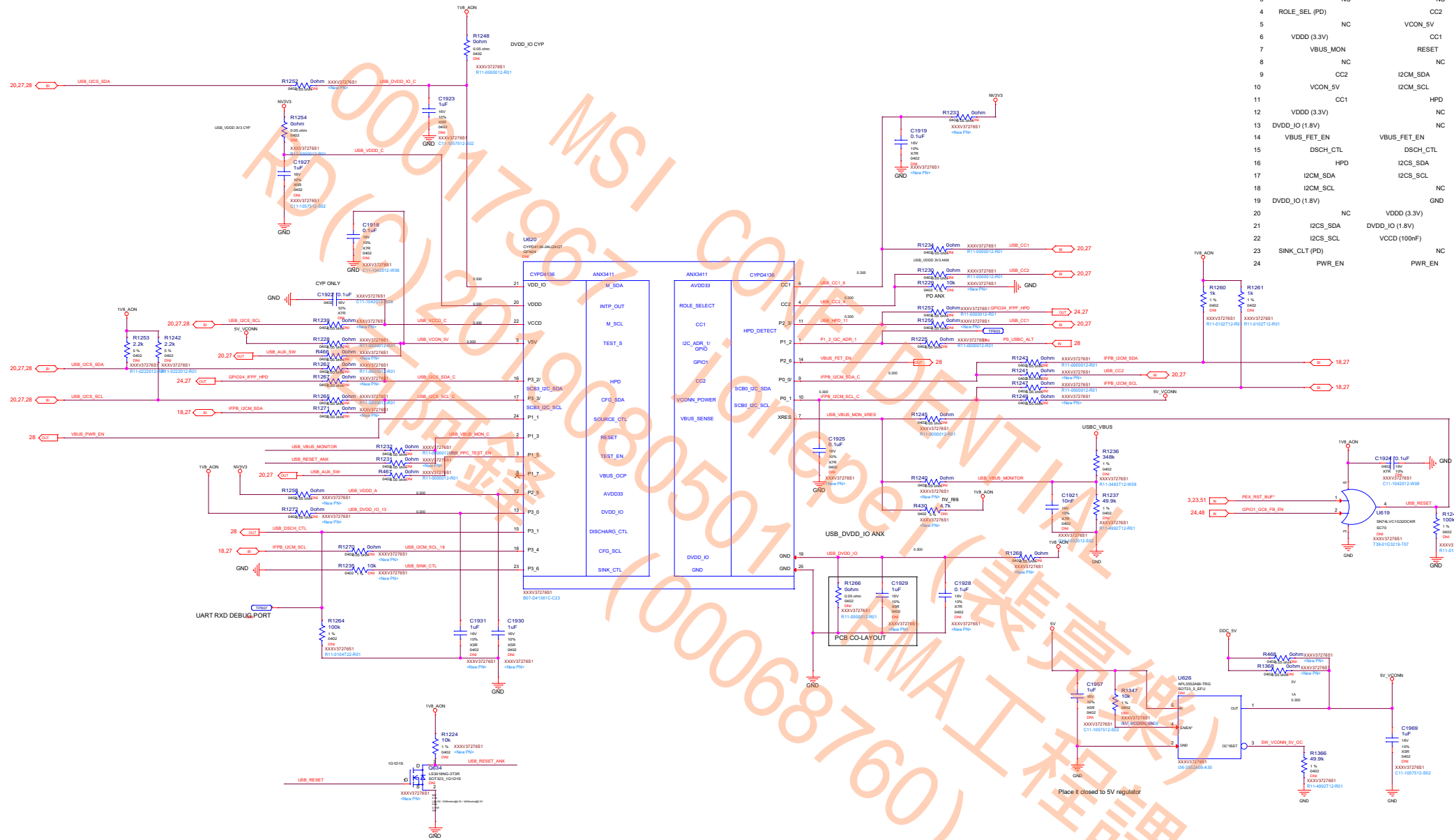
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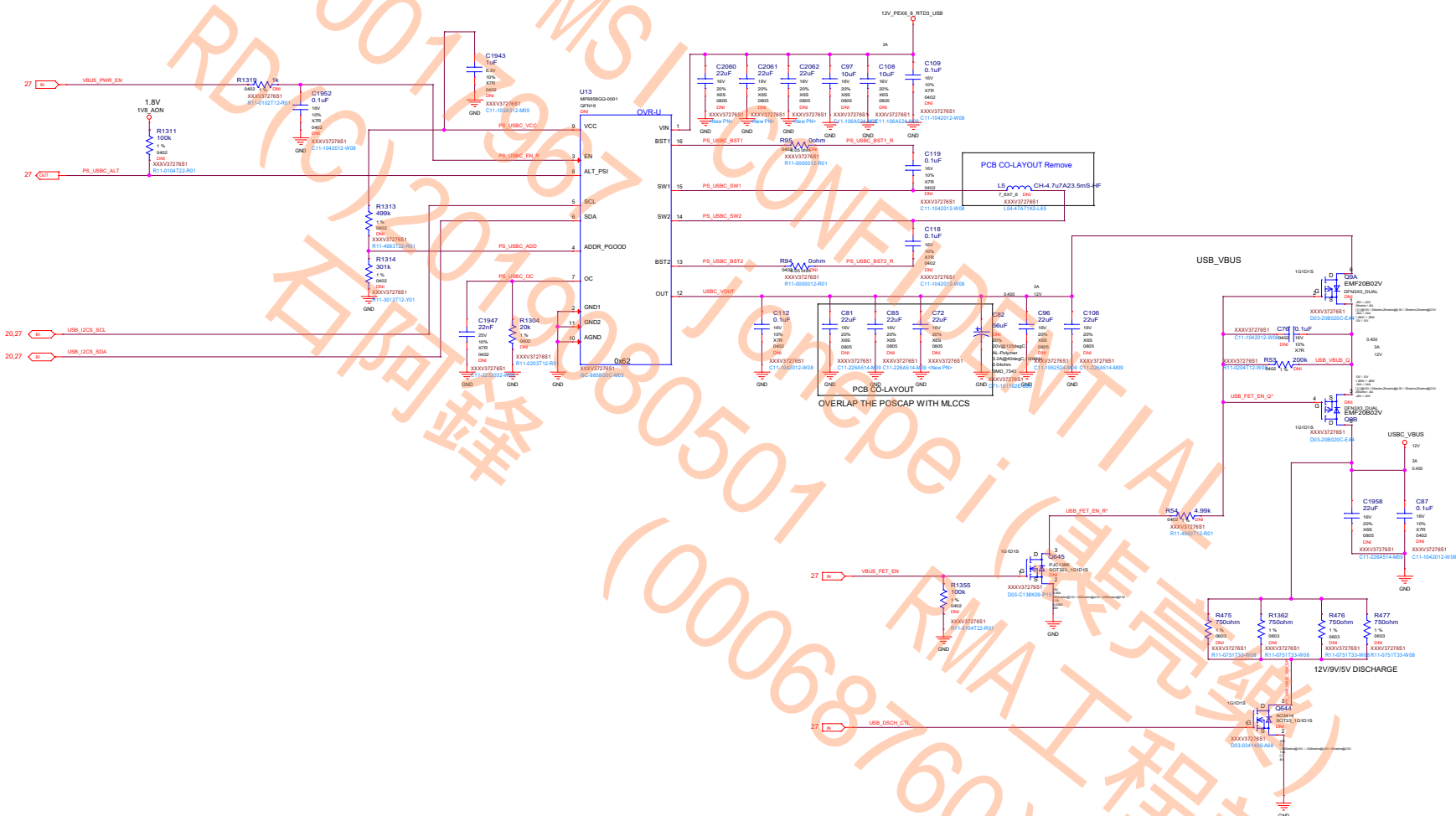
Date: Friday, November 02, 2018    Sheet: 25 of 54

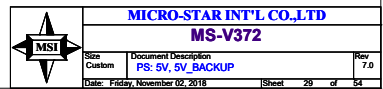
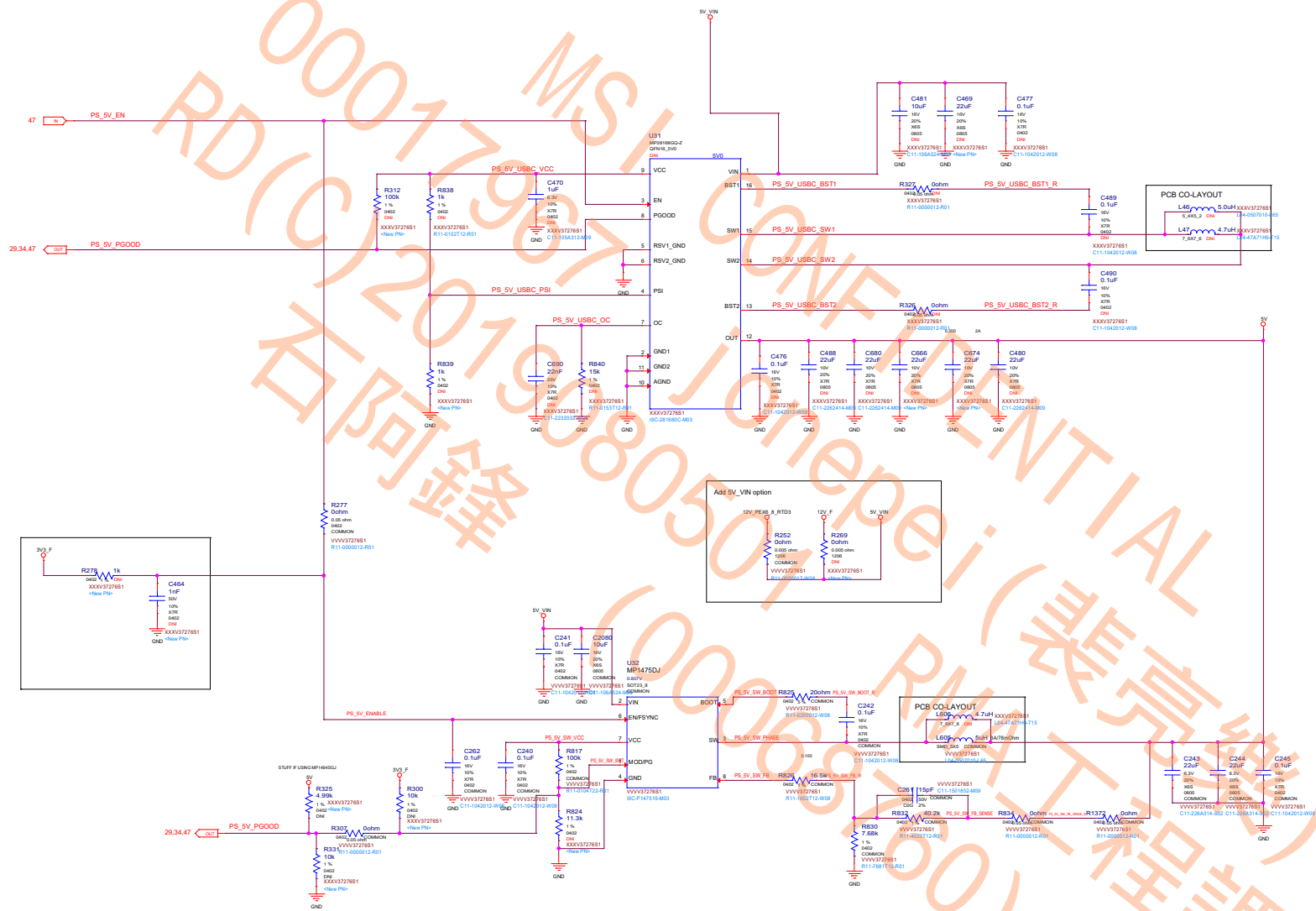


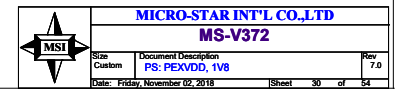
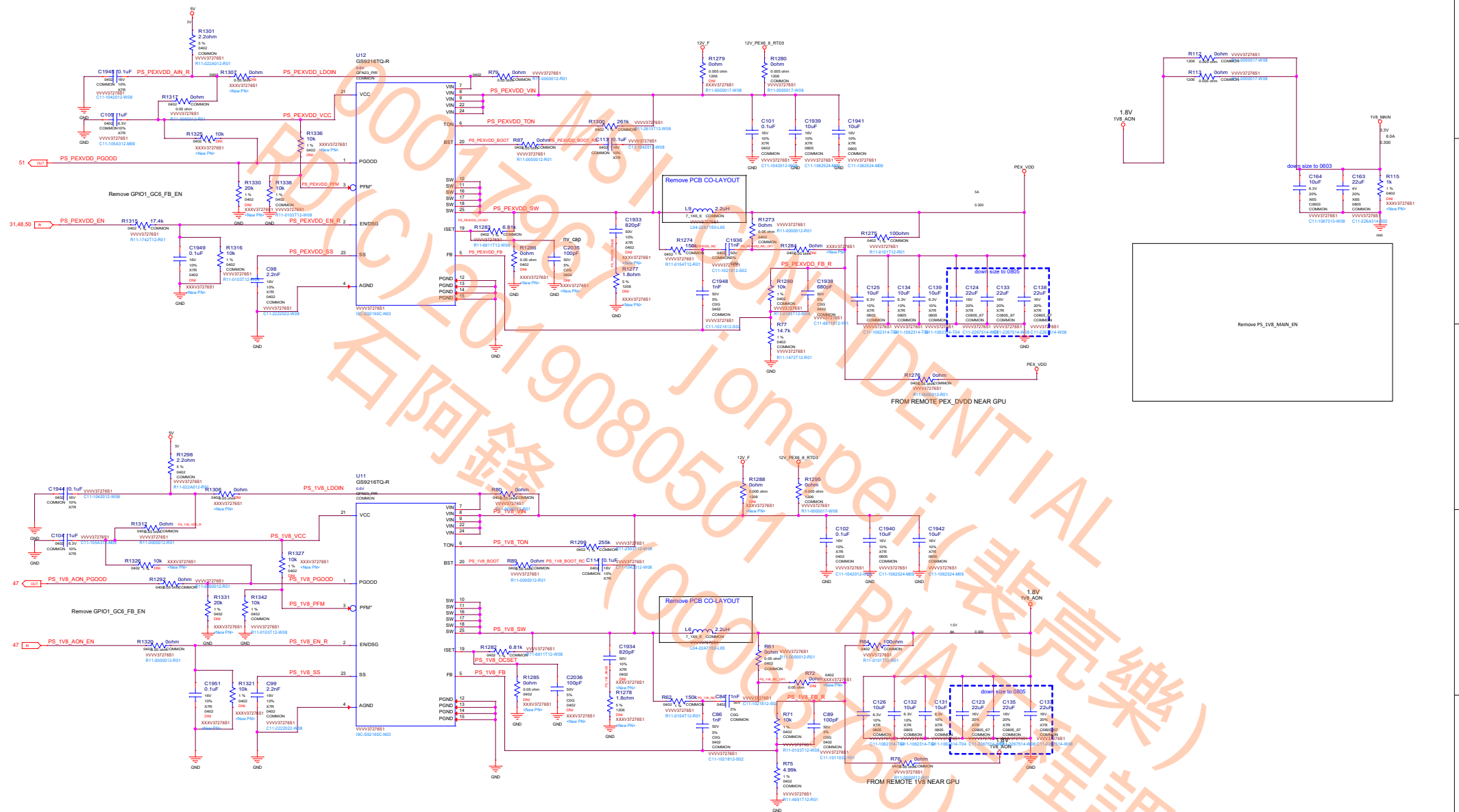




PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDD (3.3V)	OC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN





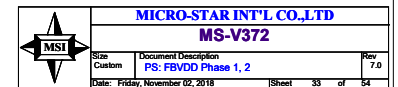
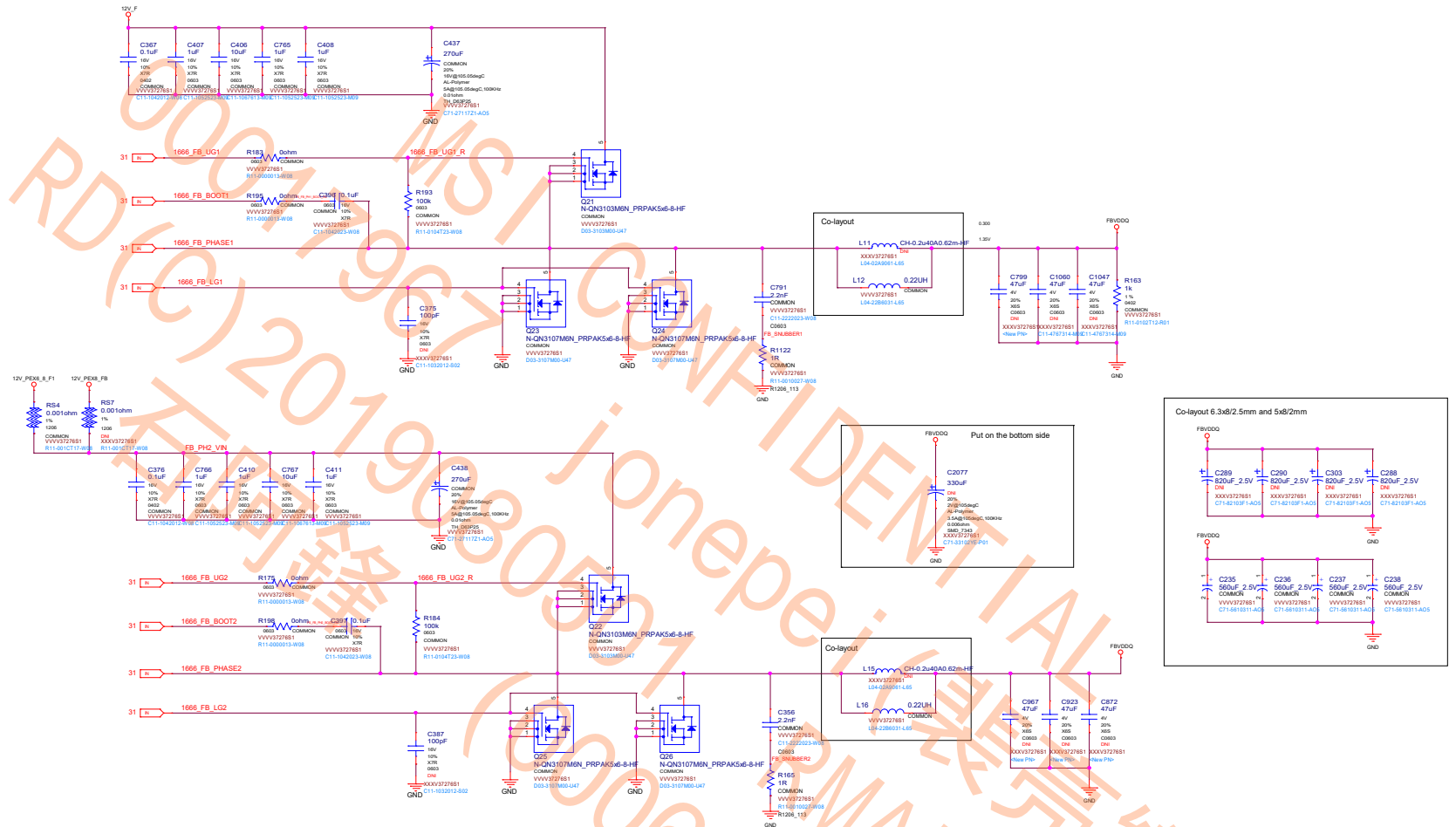




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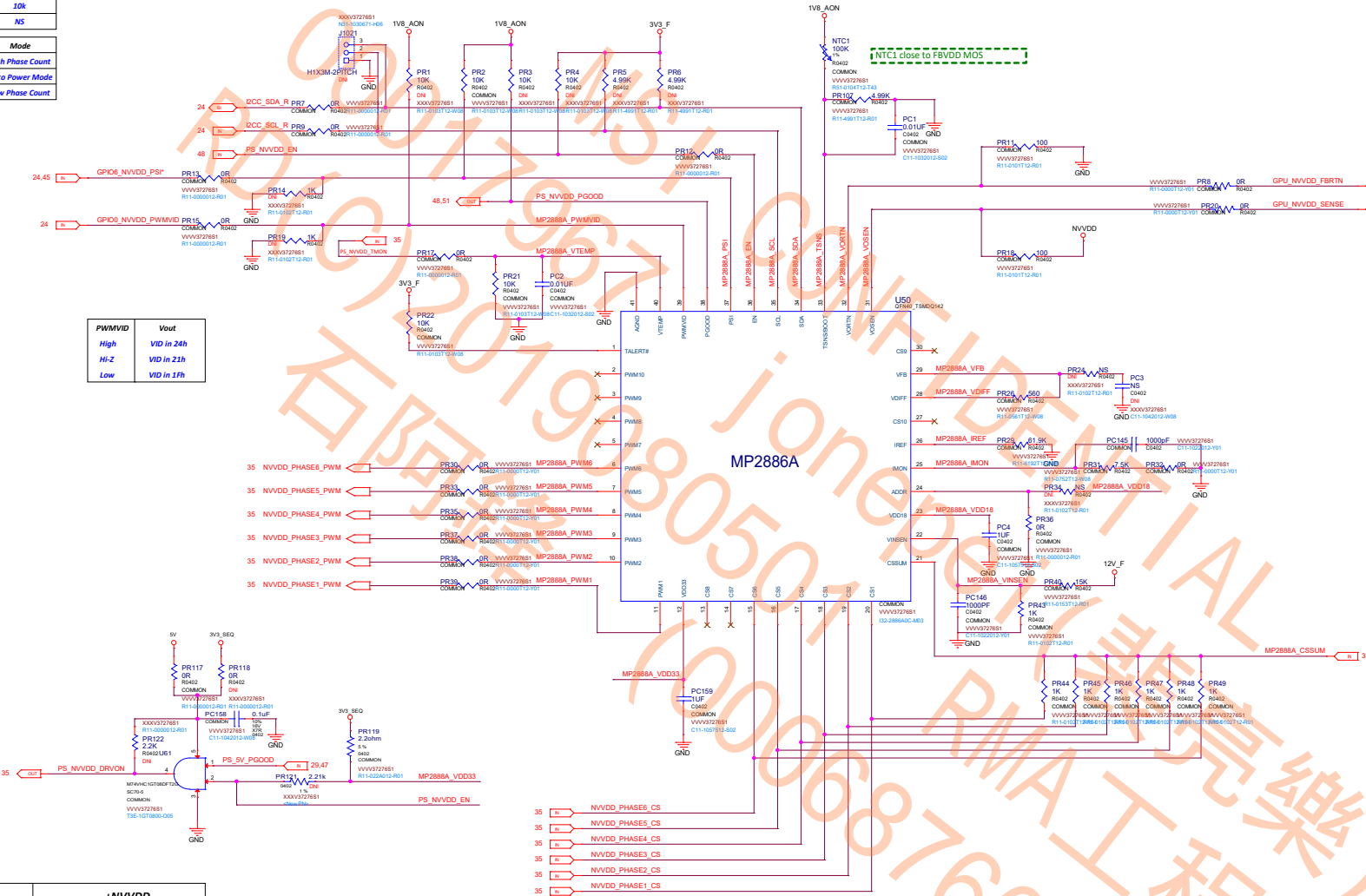
	MICRO-STAR INT'L CO.,LTD		
	MS-V372		
	Size	Document Description	Rev
	Custom	PS: FBVDD Controller OVR3 (X)	7.0
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EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

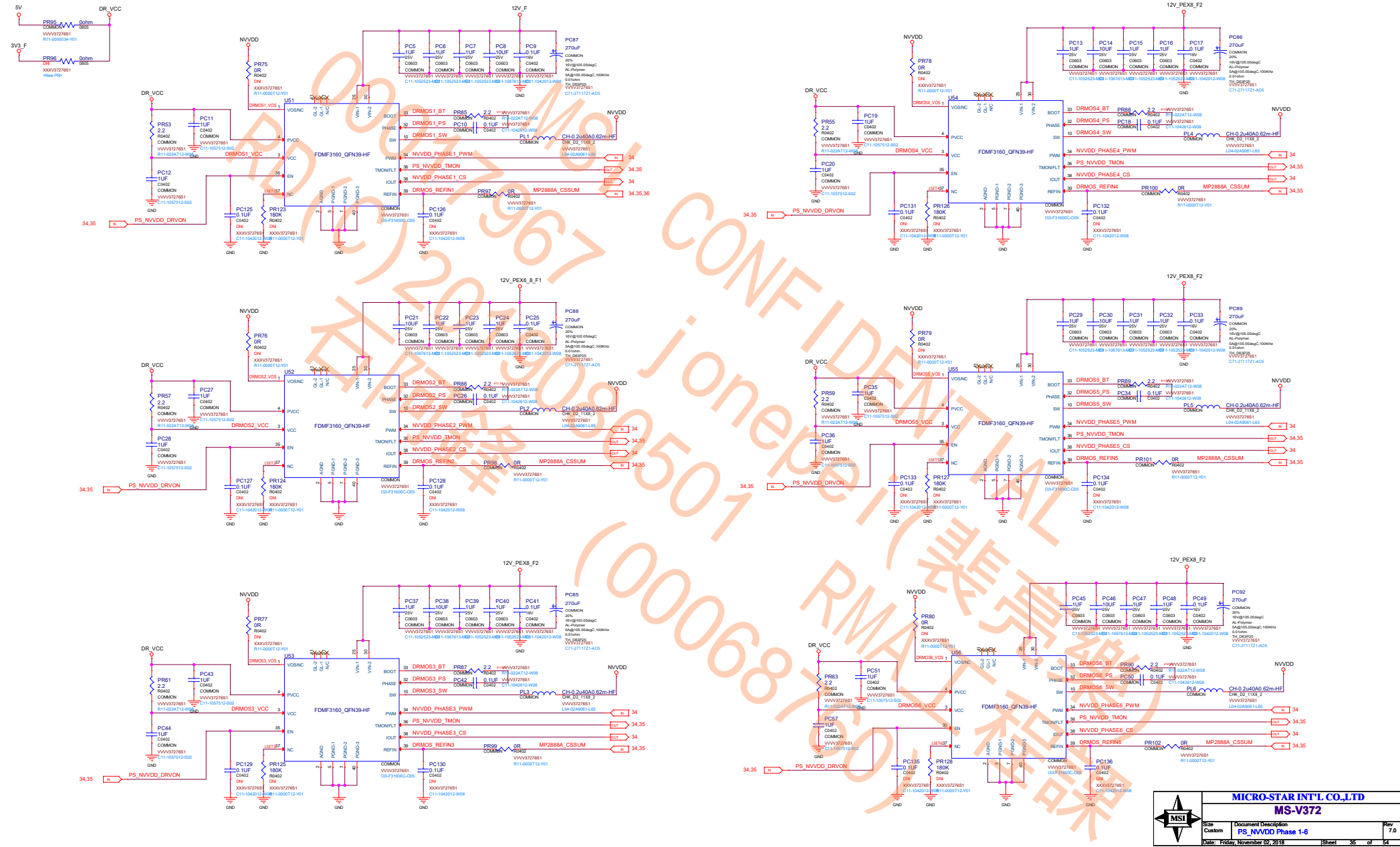


PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fr


	+NVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PSBus Address	Setting Point(V)	Rmax (kΩ) 1%	Rmax (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.099
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.84
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

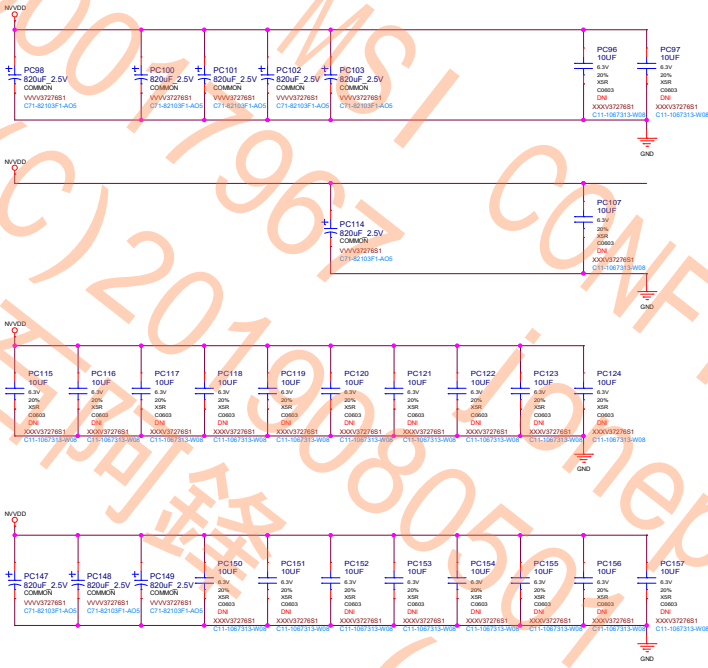
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MS-V372			
Size Custom	Document Description PS: NVDD Controller	Rev 7.0	
Date: Friday, November 02, 2018	Sheet 34	of 54	



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	MS-V372		
	Size	Document Description	Rev
	Custom	PS: NVVDD Phase(X)	7.0
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NVVDD Output CAP



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Custom	PS: NVVDD Output CAP	7.0
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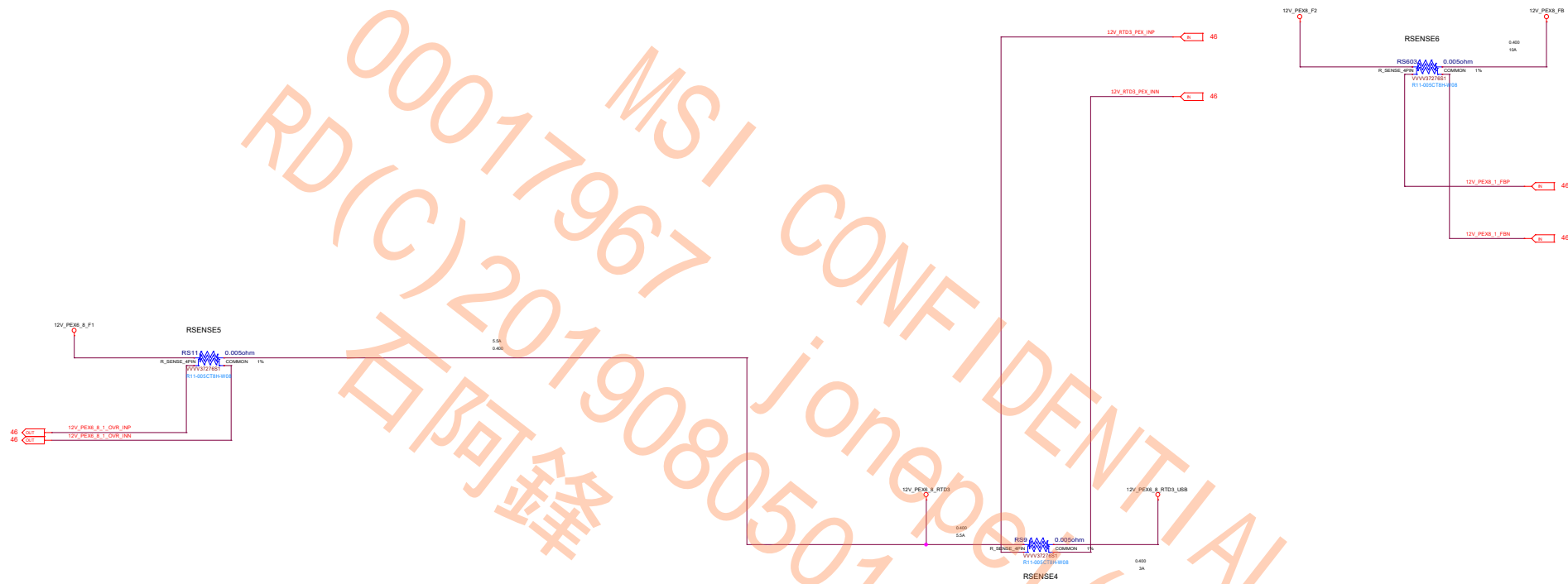
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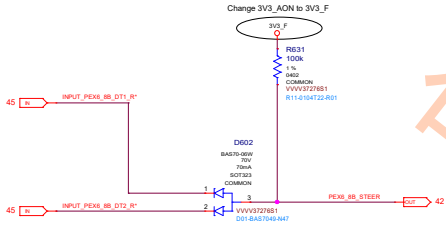
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Size	Document Description	Rev
Custom	PS:NVVDD (X)	7.0
Date: Thursday, November 01, 2018 (Sheet 38 of 54)		



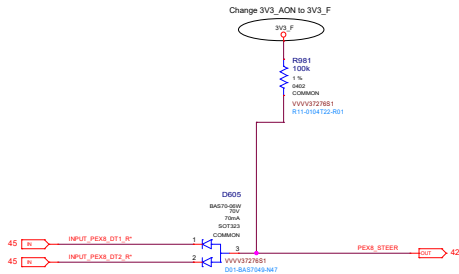
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Size	Document Description	Rev
Custom	PS: INPUT SWITCH RTD3	7.0
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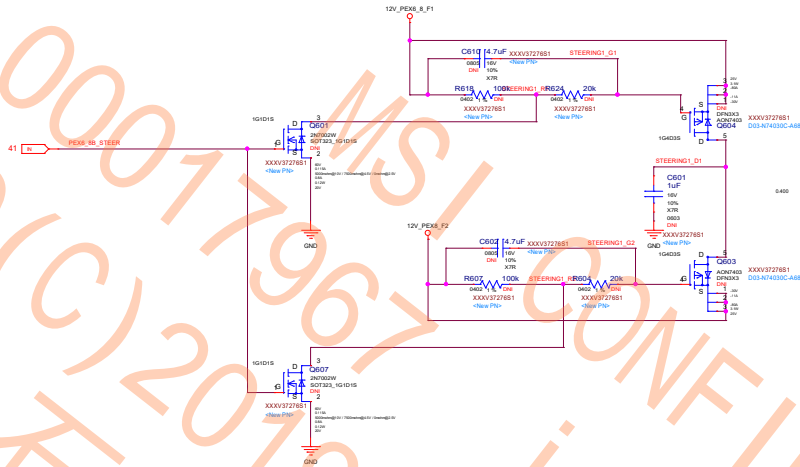




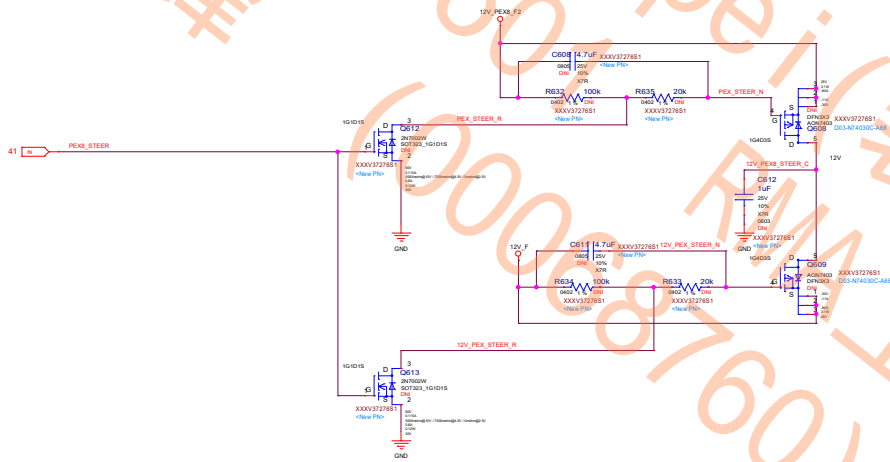
Remove 3V3\_F bypass to 3V3\_AON



12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

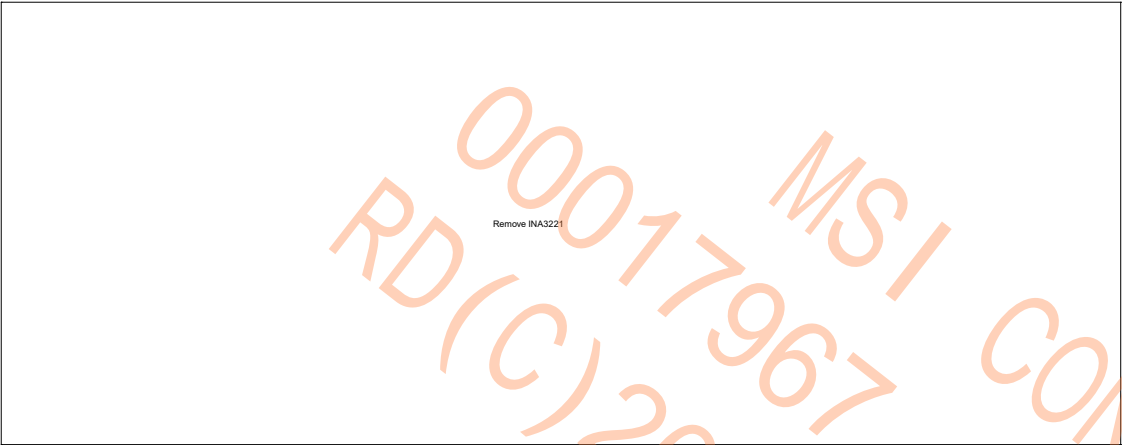


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

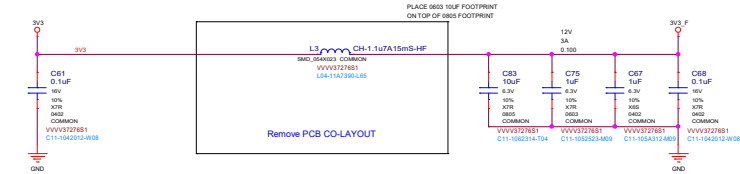


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Size	Document Description	Rev
Custom	PS: 12V CURRENT STEERING	7.0
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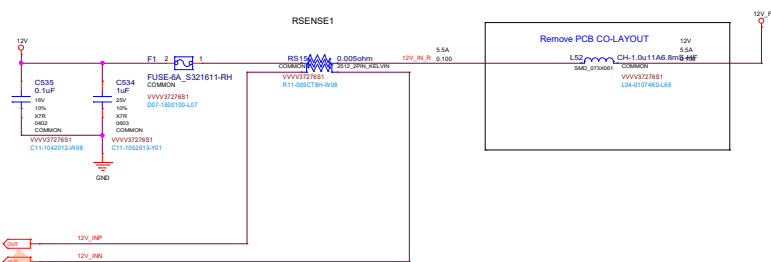
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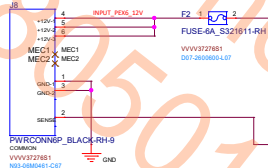
PEX 3V3 INPUT - 10W



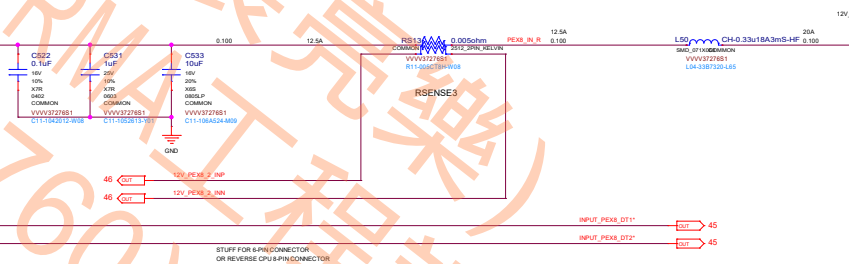
PEX\_12V INPUT - 66W



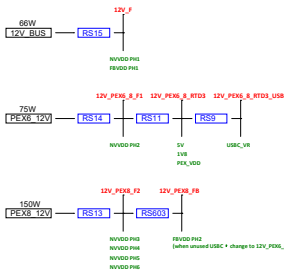
PEX6 INPUT 1 - 2x3 PCIE CON 75W

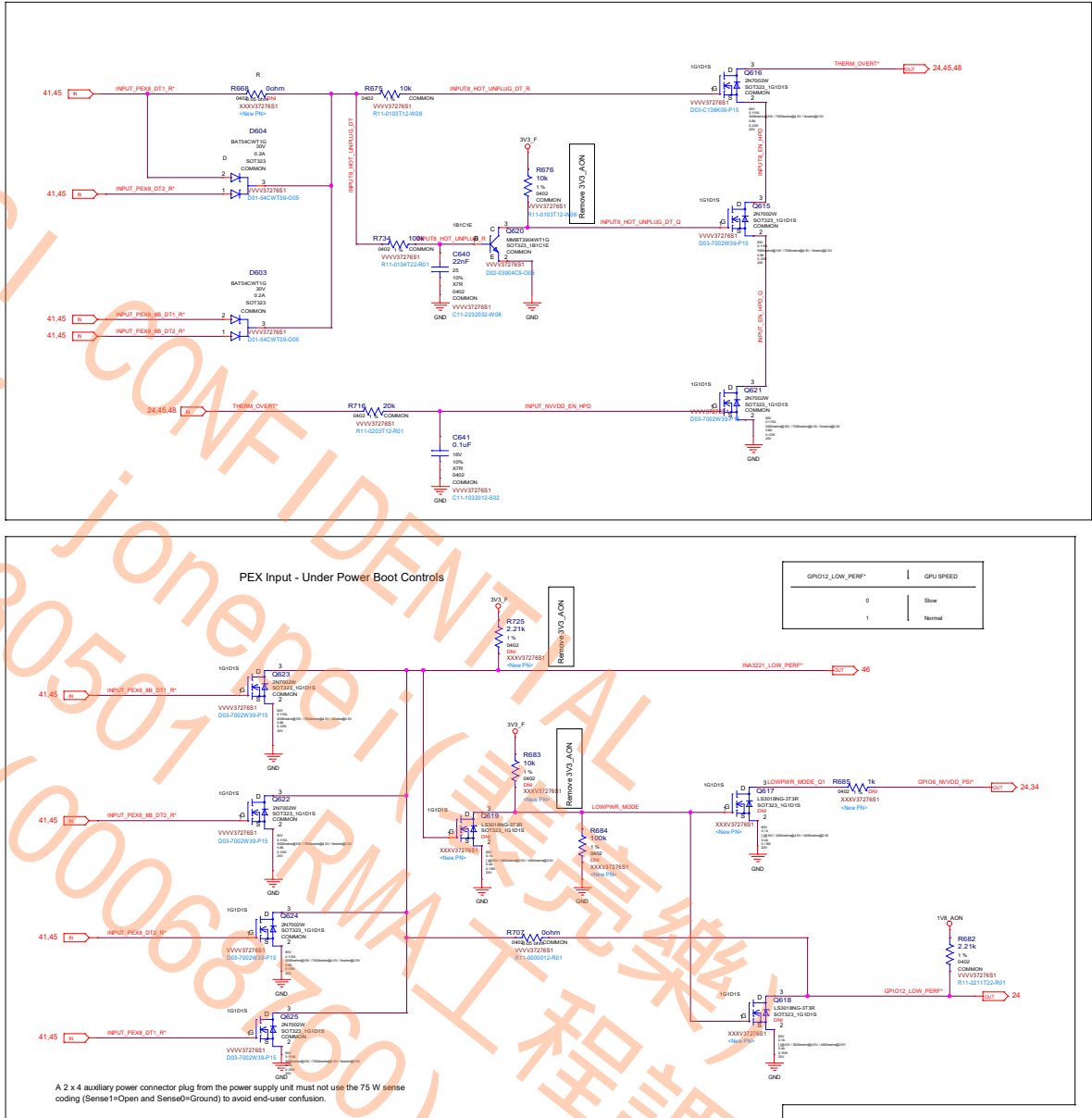
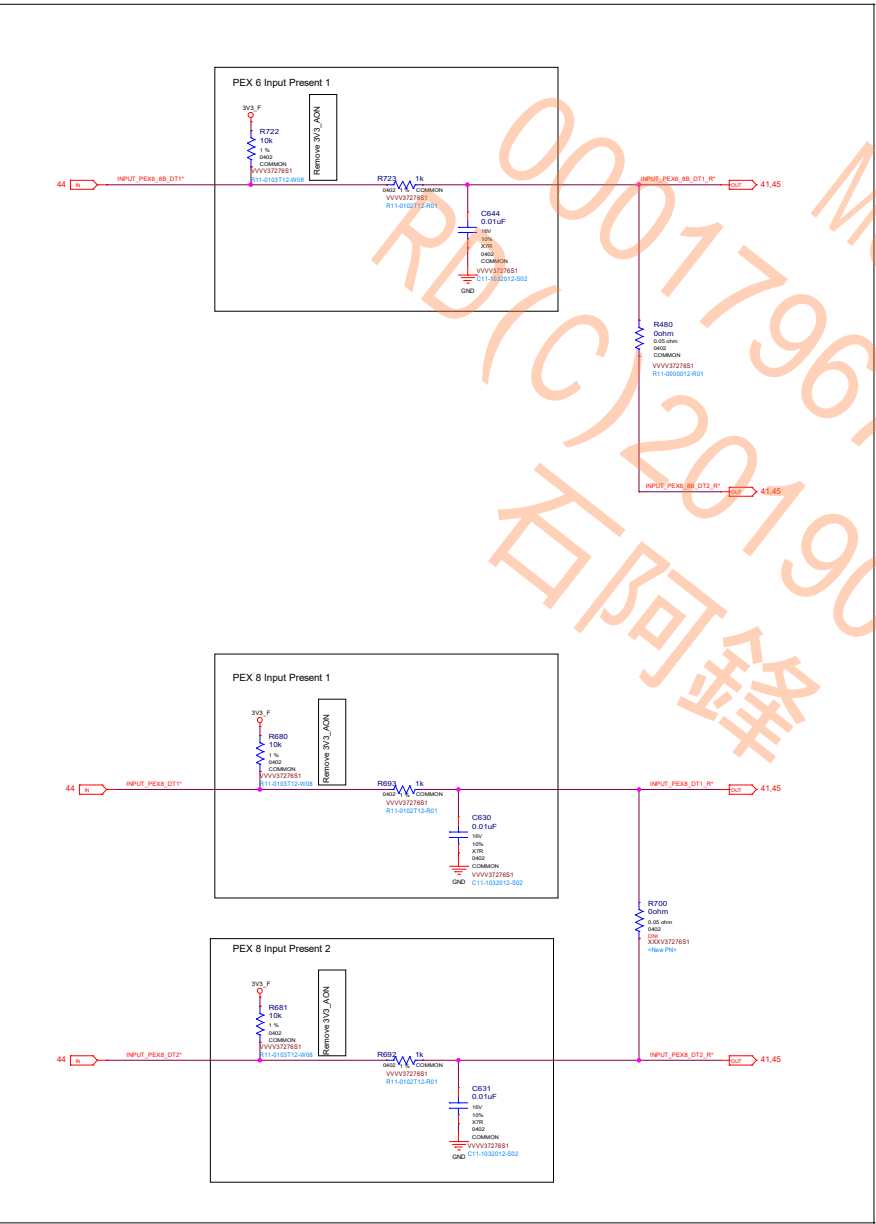


PEX8 INPUT 2 - 2x4 PCIE CON 150W

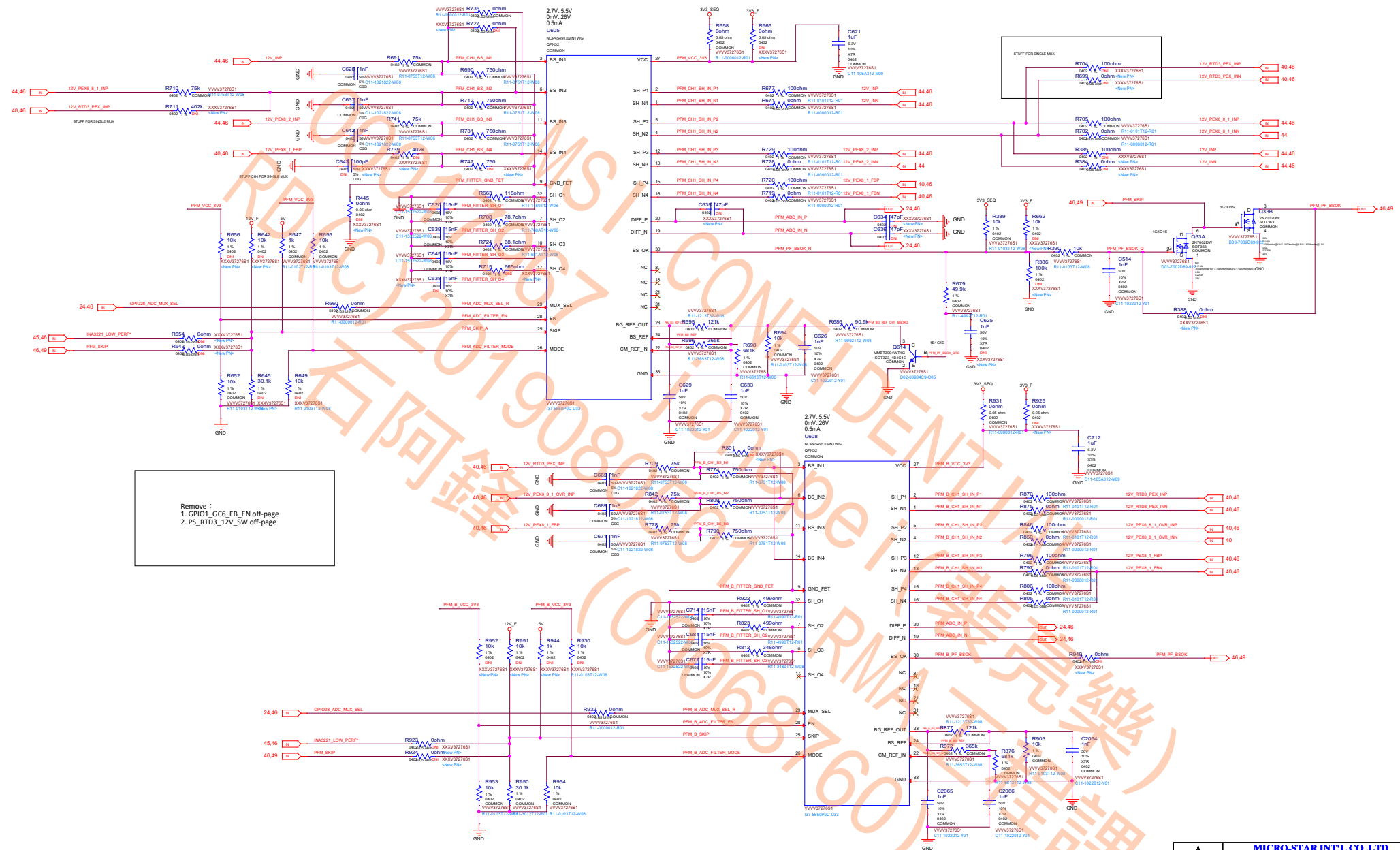


Power Topology



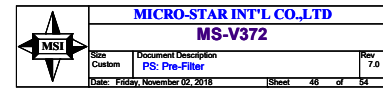


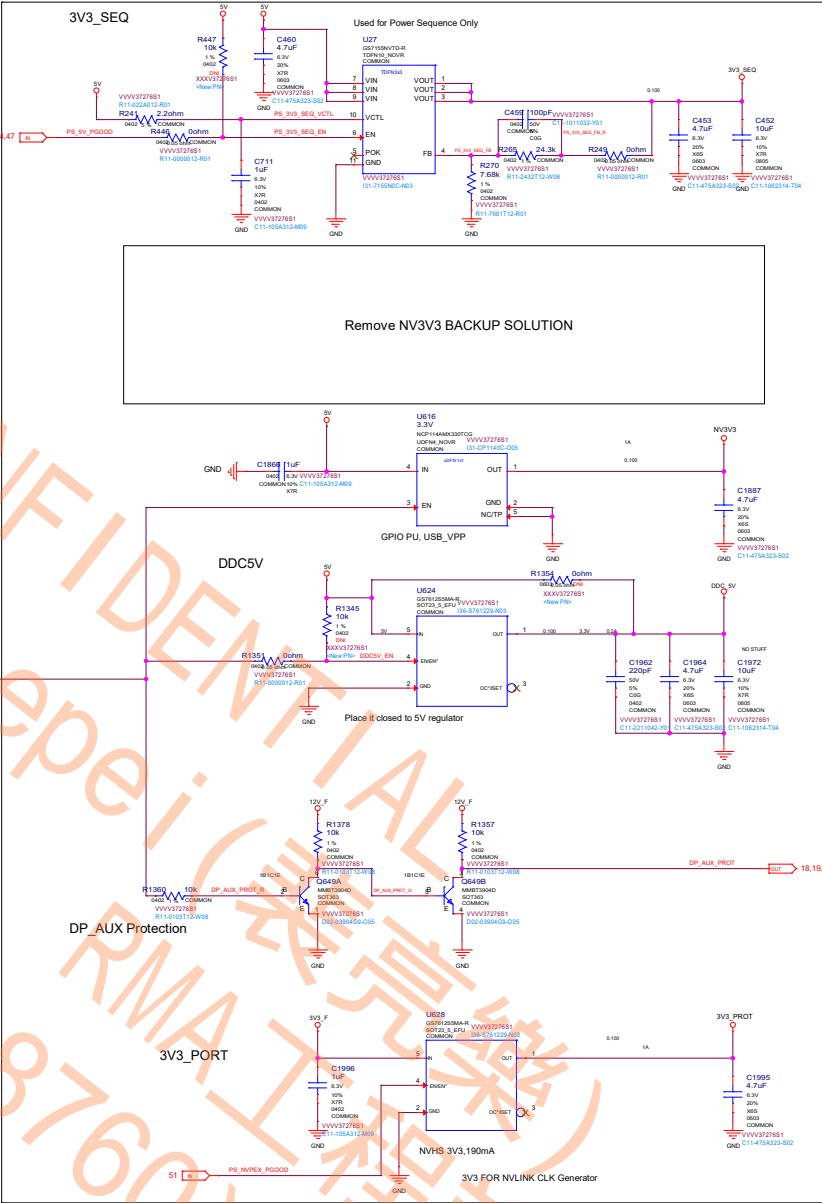
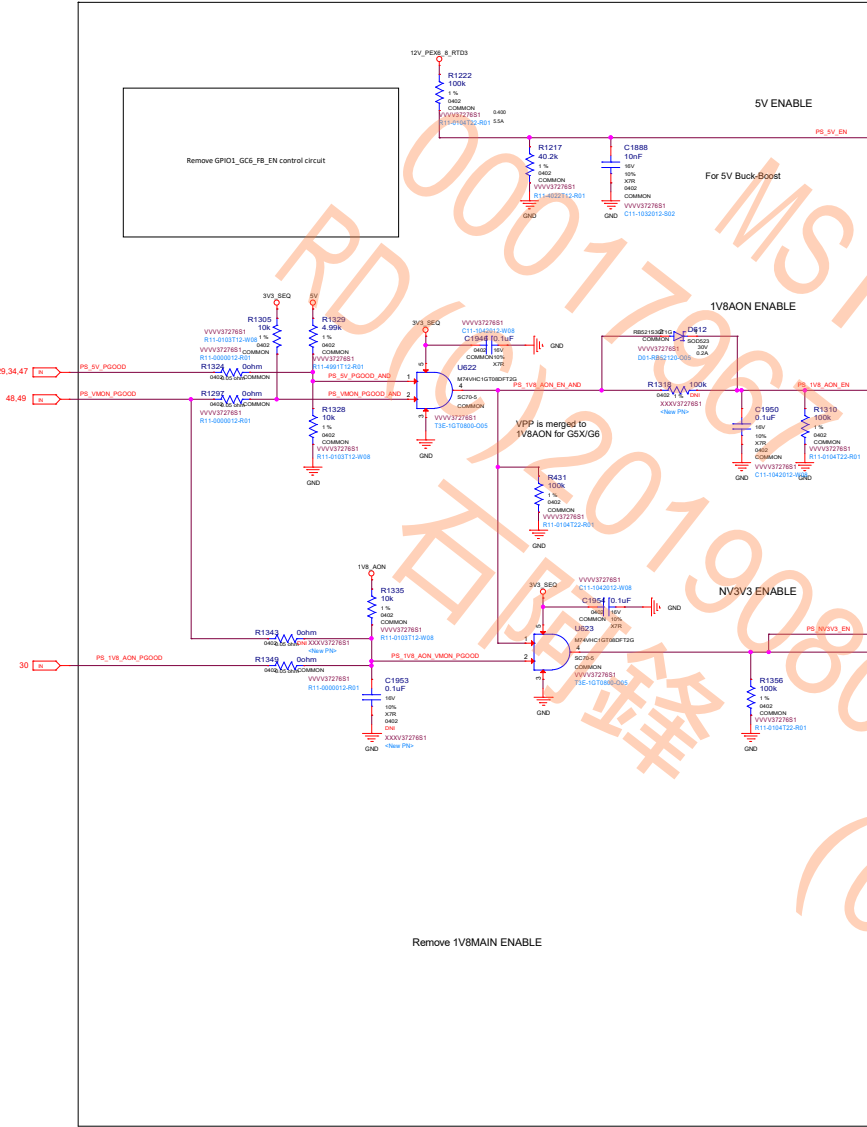


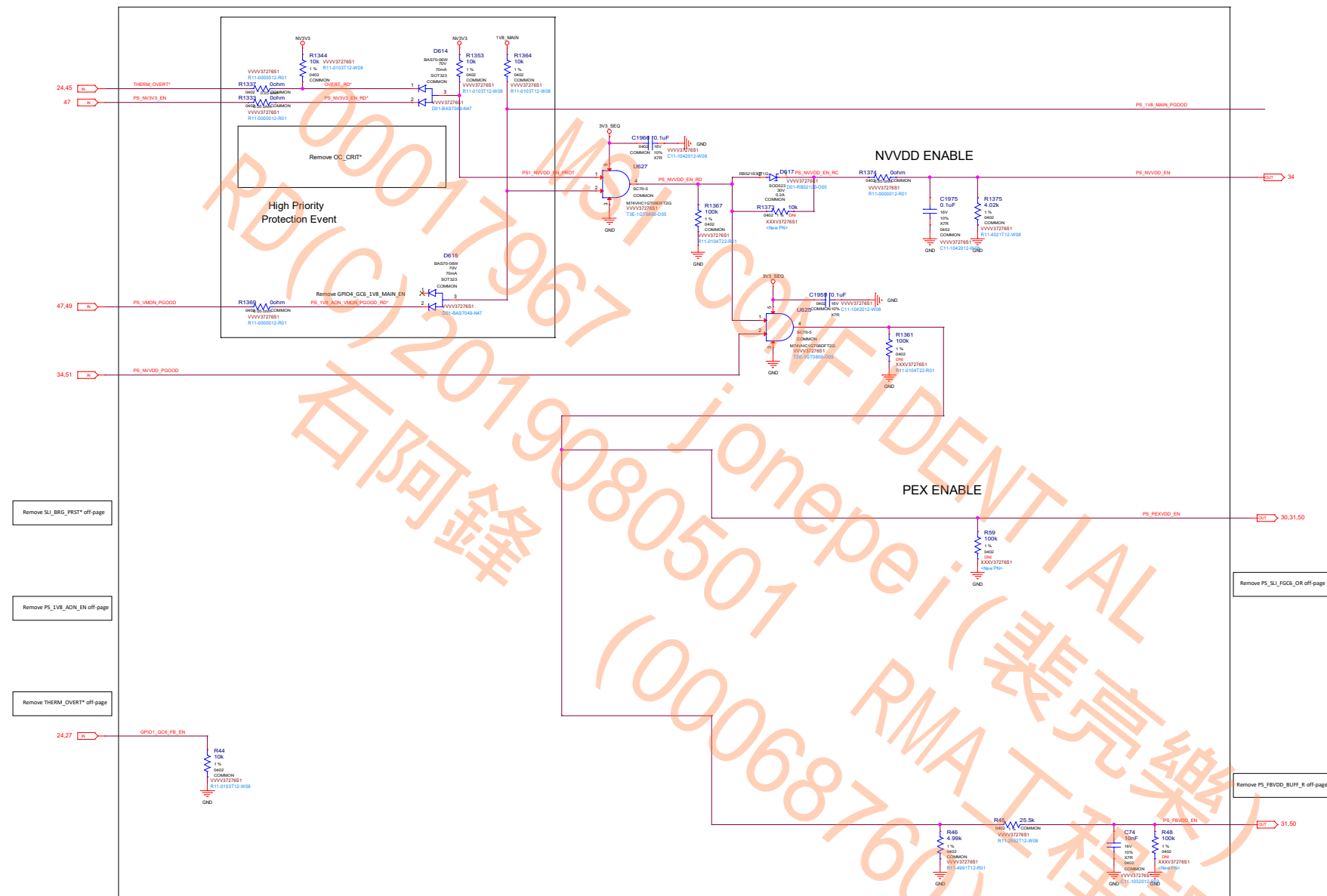


Remove :

1. GPIO1\_GC6\_FB\_EN off-page
2. PS\_RTD3\_12V\_SW off-page

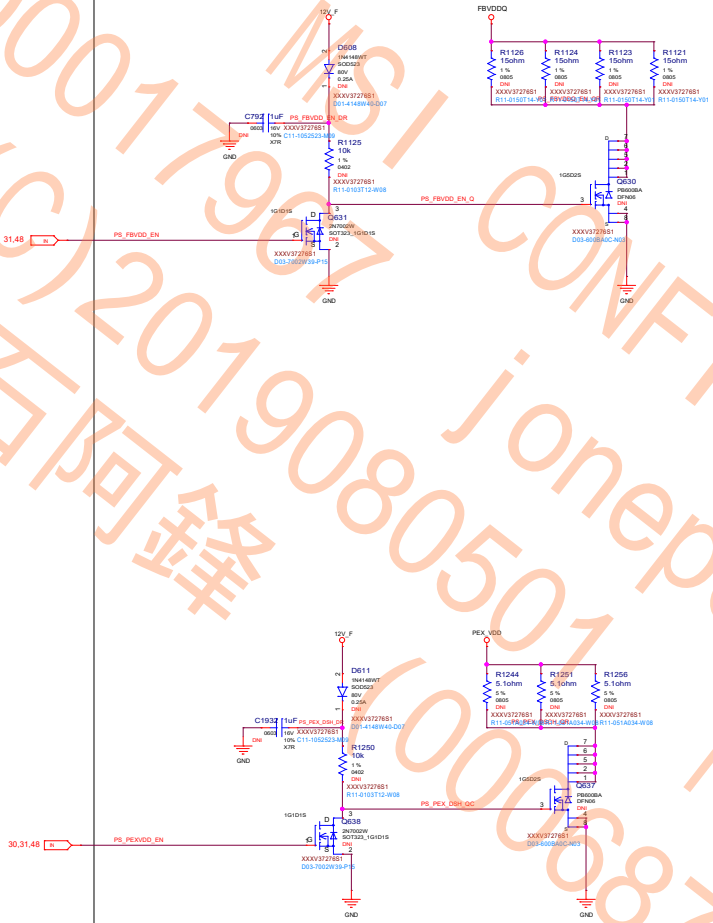


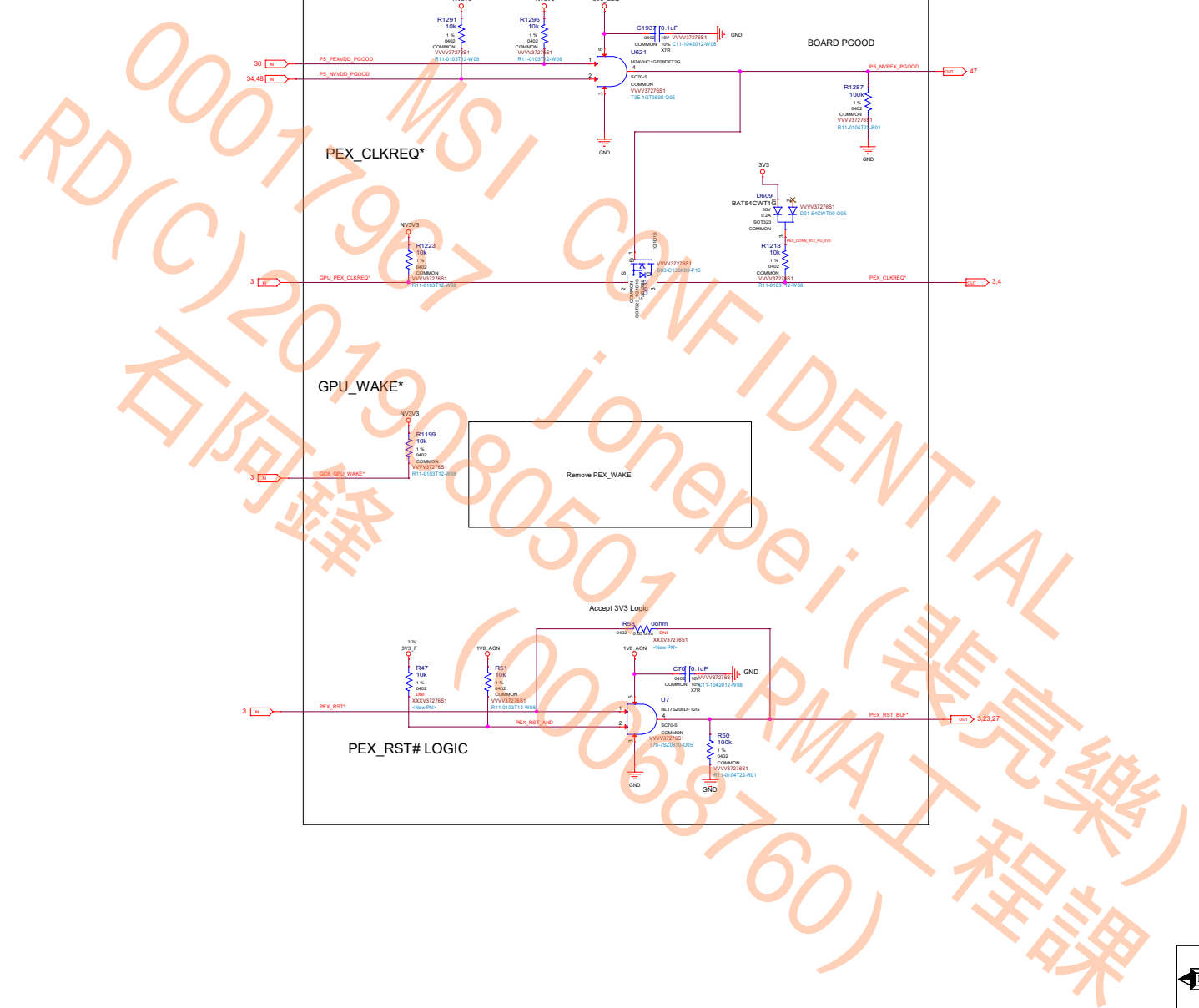




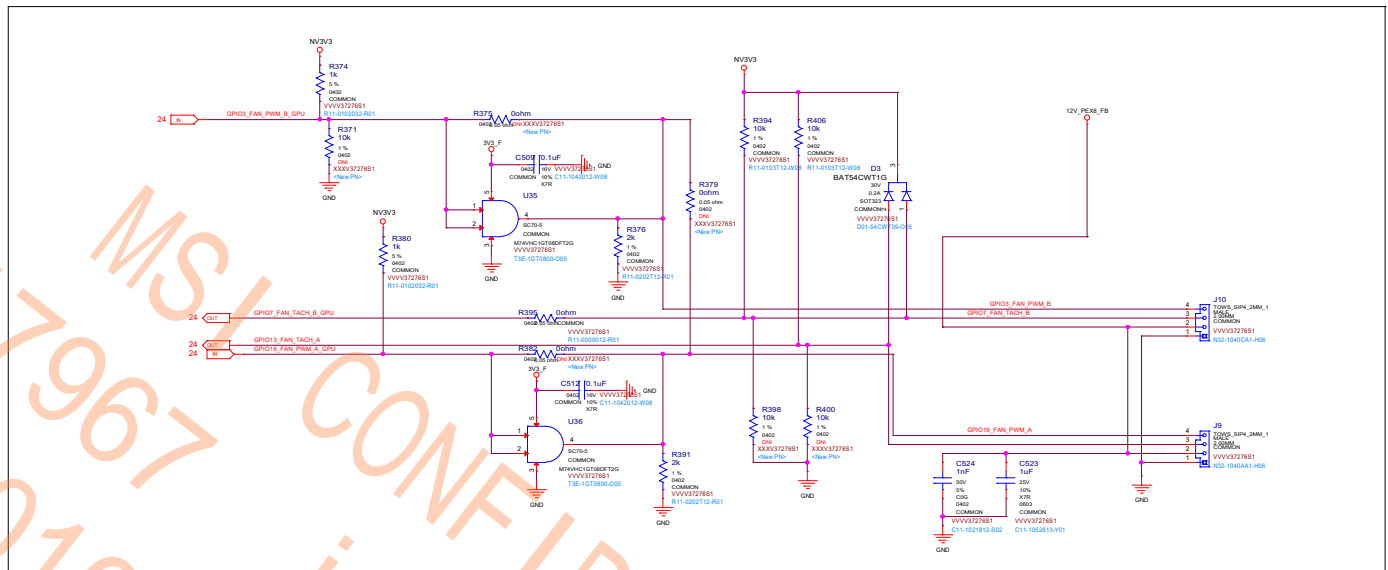
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Document Description	Rev	
SEQUENCE:NV,PEX,FB ENABLE	7.0	







Remove LED



Remove LED BOOST



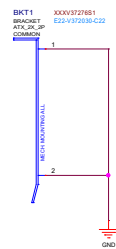
MICRO-STAR INT'L CO.,LTD			
MS-V372			
Size	Document Description	Rev	
Custom	LED & FAN HEADERS	7.0	
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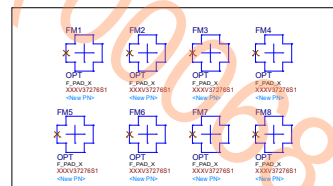
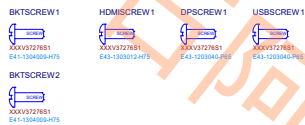
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	Custom LED_CONTROLLER_IT8295	7.0
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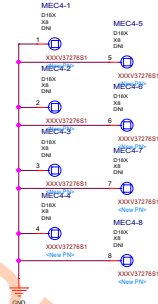
## Brackets:



## Screw



## GPU Mounting holes



## Mechanical Holes Symbol

